4.20.5 – 184 PIN PC1800/2100 DDR SDRAM UNBUFFERED DIMM DESIGN SPECIFICATION

PC1800/2100 DDR SDRAM Unbuffered DIMM

Design Specification

Revision 1.0

Table of Contents

1. Product Description

This specification defines the electrical and mechanical requirements for 184-pin, 2.5 Volt (V_{DD})/ 2.5 Volt (V_{DDQ}), Unbuffered, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR SDRAM DIMMs).These DDR DIMMs are intended for use as main memory when installed in PCs. The DDR DIMMs must permit operation with a new address every clock cycle in PC1600 and PC2100 environments.

Reference design examples are included which provide an initial basis for Unbuffered DDR DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for PC1600 and PC2100 support. All Unbuffered DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

This specification largely follows the JEDEC defined 184-pin Unbuffered DDR SDRAM DIMM product. (Refer to JEDEC standard JESD21-C, Section 4.5.10, at www.jedec.org).

Product Family Attributes

DIMM Organization	x64, x72 ECC	Notes
DIMM Dimensions (max)	5.256” x 1.256” x 0.157”	
Pin Count	184	
DDR SDRAMs Supported	64Mb, 128Mb, 256Mb, 512Mb	
Capacity	32MB - 1GB	
Serial PD	Consistent with JEDEC JC 42.5 Item 849A	
Voltage Options	2.5 Volt V_{DD}/V_{DDQ} 2.5 Volt to 3.3 Volt V_{DD} SPD	All DDR modules use a common V_{DD}-V_{DDQ} power plane. They are tid together on the DIMM, but by standard definition are supported on the pinout to accommodate future enhancements.
Interface	SSTL_2	
Note 1: V_{DD} SPD is not tied to V_{DD} or V_{DDQ} on the DDR DIMM.		

2. Environmental Requirements

184-pin Unbuffered DDR SDRAM DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +55	∝C	1
H_{OPR}	Operating Humidity (relative)	10 to 90	%	1
T_{STG}	Storage Temperature	-50 to +100	∝C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.

3. Architecture

Pin Description

Pin Name	Description		Pin Name	Description
A0 - A13	SDRAM address bus		CK0 - CK2	SDRAM clock (positive lines of 3 differential pairs)
BA0 - BA1	SDRAM bank select		$\overline{CK0}$ - $\overline{CK2}$	SDRAM clock (negative lines of these three pairs)
DQ0 - DQ63	DIMM memory data bus		SCL	IIC serial bus clock for EEPROM
CB0 - CB7	DIMM ECC check bits		SDA	IIC serial bus data line for EEPROM
/RAS	SDRAM row address strobe		SA0 - SA2	IIC slave address select for EEPROM
/CAS	SDRAM column address strobe		VDD*	SDRAM positive power supply
/WE	SDRAM write strobe		VDDQ*	SDRAM I/O Driver positive power supply
/S0 - /S1	SDRAM chip select lines (Phys. banks 0 and 1)		VREF	SDRAM I/O reference supply
CKE0 - CKE1	SDRAM clock enable lines		VSS	Power supply return (ground)
DQS0 - DQS8	SDRAM low data strobes		VDDSPD	Serial EEPROM positive power supply (2.5 Volts to 3.3 Volts)--VDDSPD is not connected to VDD or VDDQ
DM(0-8)/DQS(9-17)	SDRAM low data masks/high data strobes (x4, 2 Phys. banks)		NC	Spare pins (no connect)
VDDID	VDD identification flag			

*The VDD and VDDQ pins are tied to the single power-plane on theee designs. See page 35.

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0 - CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs. All the DDR SDRAM addr/cntl inputs are sampled on the rising edge of their associated clocks.
$\overline{CK0}$ - $\overline{CK2}$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{S0}$, $\overline{S1}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL2 inputs.
V_{DDQ}	Supply		Power supply for the DDR SDRAM output buffers to provide improved noise immunity. For all current DDR unbuffered DIMM designs, VDDQ shares the same power plane as VDD pins.
BA0,1	(SSTL)	—	Selects which SDRAM bank of four is activated.
A0 - A9 A10/AP, A11-A13	(SSTL)	—	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-12 defines the column address (CA0-CA12) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ63, CB0 - CB7	(SSTL)	—	Data and Check Bit Input/Output pins.
DM0-DM8	(SSTL)	Active High	Masks write data when high, issued concurrently with input data. Both DM and DQ have a write latency of one clock once the write command is registered into the SDRAM.
V_{DD}, V_{DD} SPD V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers, core logic and Signal Presence Detect.
DQS0-DQS8	(SSTL)	Negative and Positive Edge	Data strobe for input and output data. For the x16, LDQS corresponds to the data on DQ0-7, VDQs corresponds to the data on DQ8-15.
SA0 - 2		—	These signals are tied at the system planar to either V_{SS} or V_{DD} to configure the serial SPD EEPROM address range.
SDA		—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pullup.
SCL		—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pullup.

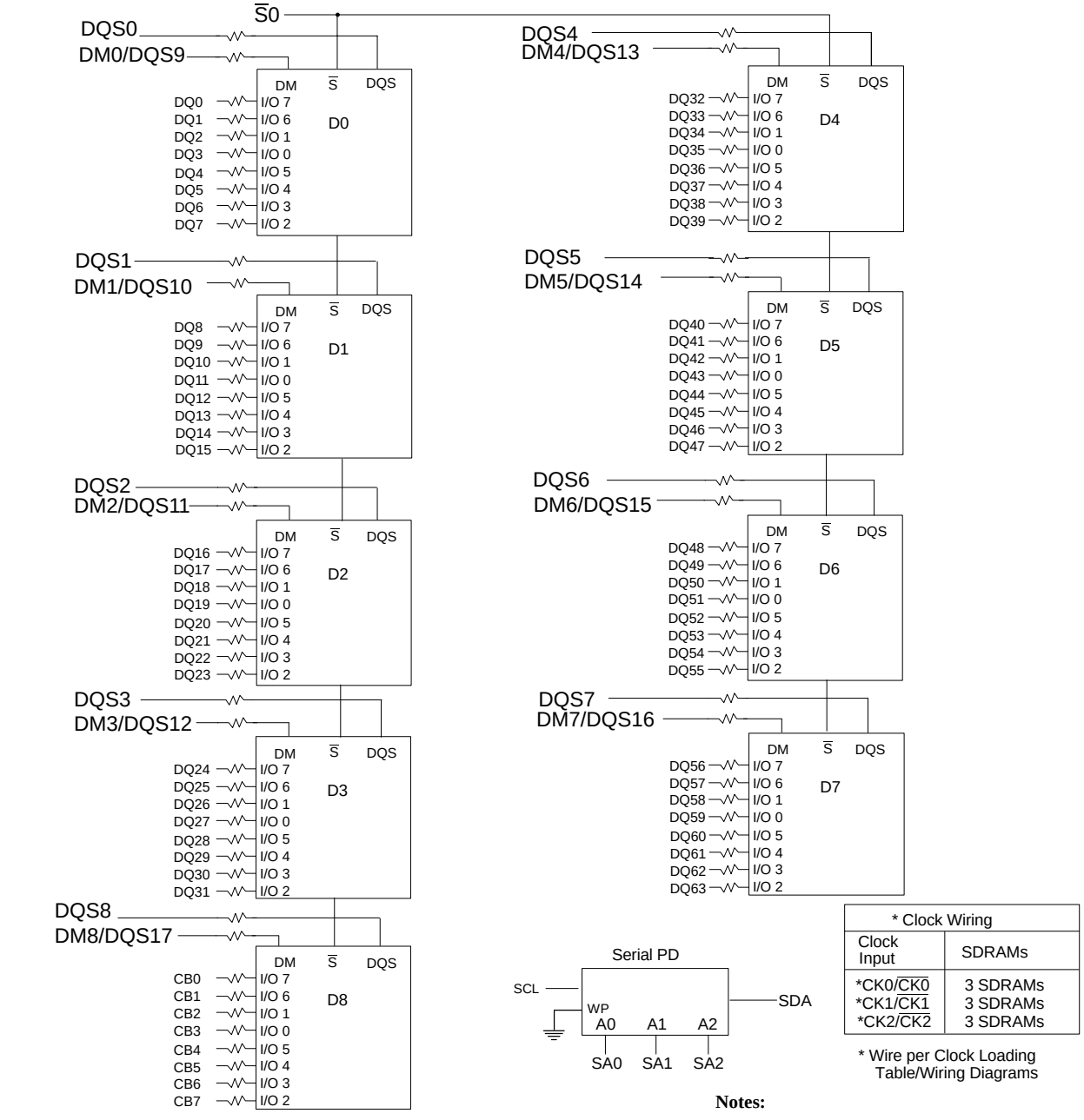
184-Pin DDR SDRAM DIMM Pin Assignments

Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 -144, right side 145 -184)			Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 -144, right side 145 -184)		
Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC
1	VREF	VREF	93	VSS	VSS	48	A0	A0	140	NC	DM8/DQS17
2	DQ0	DQ0	94	DQ4	DQ4	49	NC	CB2	141	A10	A10
3	VSS	VSS	95	DQ5	DQ5	50	VSS	VSS	142	NC	CB6
4	DQ1	DQ1	96	VDDQ	VDDQ	51	NC	CB3	143	VDDQ	VDDQ
5	DQS0	DQS0	97	DM0/DQS9	DM0/DQS9	52	BA1	BA1	144	NC	CB7
6	DQ2	DQ2	98	DQ6	DQ6	KEY			KEY		
7	VDD	VDD	99	DQ7	DQ7	53	DQ32	DQ32	145	VSS	VSS
8	DQ3	DQ3	100	VSS	VSS	54	VDDQ	VDDQ	146	DQ36	DQ36
9	NC	NC	101	NC	NC	55	DQ33	DQ33	147	DQ37	DQ37
10	NC	NC	102	NC	NC	56	DQS4	DQS4	148	VDD	VDD
11	VSS	VSS	103	A13	A13	57	DQ34	DQ34	149	DM4/DQS13	DM4/DQS13
12	DQ8	DQ8	104	VDDQ	VDDQ	58	VSS	VSS	150	DQ38	DQ38
13	DQ9	DQ9	105	DQ12	DQ12	59	BA0	BA0	151	DQ39	DQ39
14	DQS1	DQS1	106	DQ13	DQ13	60	DQ35	DQ35	152	VSS	VSS
15	VDDQ	VDDQ	107	DM1/DQS10	DM1/DQS10	61	DQ40	DQ40	153	DQ44	DQ44
16	CK1	CK1	108	VDD	VDD	62	VDDQ	VDDQ	154	/RAS	/RAS
17	/CK1	/CK1	109	DQ14	DQ14	63	/WE	/WE	155	DQ45	DQ45
18	VSS	VSS	110	DQ15	DQ15	64	DQ41	DQ41	156	VDDQ	VDDQ
19	DQ10	DQ10	111	CKE1	CKE1	65	/CAS	/CAS	157	/S0	/S0
20	DQ11	DQ11	112	VDDQ	VDDQ	66	VSS	VSS	158	/S1	/S1
21	CKE0	CKE0	113	BA2	BA2	67	DQS5	DQS5	159	DM5/DQS14	DM5/DQS14
22	VDDQ	VDDQ	114	DQ20	DQ20	68	DQ42	DQ42	160	VSS	VSS
23	DQ16	DQ16	115	A12	A12	69	DQ43	DQ43	161	DQ46	DQ46
24	DQ17	DQ17	116	VSS	VSS	70	VDD	VDD	162	DQ47	DQ47
25	DQS2	DQS2	117	DQ21	DQ21	71	NC, /S2	NC, /S2	163	NC, /S3	NC, /S3
26	VSS	VSS	118	A11	A11	72	DQ48	DQ48	164	VDDQ	VDDQ
27	A9	A9	119	DM2/DQS11	DM2/DQS11	73	DQ49	DQ49	165	DQ52	DQ52
28	DQ18	DQ18	120	VDD	VDD	74	VSS	VSS	166	DQ53	DQ53
29	A7	A7	121	DQ22	DQ22	75	/CK2	/CK2	167	NC, FETEN	NC, FETEN
30	VDDQ	VDDQ	122	A8	A8	76	CK2	CK2	168	VDD	VDD
31	DQ19	DQ19	123	DQ23	DQ23	77	VDDQ	VDDQ	169	DM6/DQS15	DM6/DQS15
32	A5	A5	124	VSS	VSS	78	DQS6	DQS6	170	DQ54	DQ54
33	DQ24	DQ24	125	A6	A6	79	DQ50	DQ50	171	DQ55	DQ55
34	VSS	VSS	126	DQ28	DQ28	80	DQ51	DQ51	172	VDDQ	VDDQ
35	DQ25	DQ25	127	DQ29	DQ29	81	VSS	VSS	173	NC	NC
36	DQS3	DQS3	128	VDDQ	VDDQ	82	VDDID	VDDID	174	DQ60	DQ60
37	A4	A4	129	DM3/DQS12	DM3/DQS12	83	DQ56	DQ56	175	DQ61	DQ61
38	VDD	VDD	130	A3	A3	84	DQ57	DQ57	176	VSS	VSS
39	DQ26	DQ26	131	DQ30	DQ30	85	VDD	VDD	177	DM7/DQS16	DM7/DQS16
40	DQ27	DQ27	132	VSS	VSS	86	DQS7	DQS7	178	DQ62	DQ62
41	A2	A2	133	DQ31	DQ31	87	DQ58	DQ58	179	DQ63	DQ63
42	VSS	VSS	134	NC	CB4	88	DQ59	DQ59	180	VDDQ	VDDQ
43	A1	A1	135	NC	CB5	89	VSS	VSS	181	SA0	SA0
44	NC	CB0	136	VDDQ	VDDQ	90	NC	NC	182	SA1	SA1
45	NC	CB1	137	CK0	CK0	91	SDA	SDA	183	SA2	SA2
46	VDD	VDD	138	/CK0	/CK0	92	SCL	SCL	184	VDDSPD	VDDSPD
47	NC	DQS8	139	VSS	VSS						

NC = No Connect NU = Not Useable

Block Diagram: Raw Card Version A, x72

(Populated as 1 physical bank of x8 DDR SDRAMs)

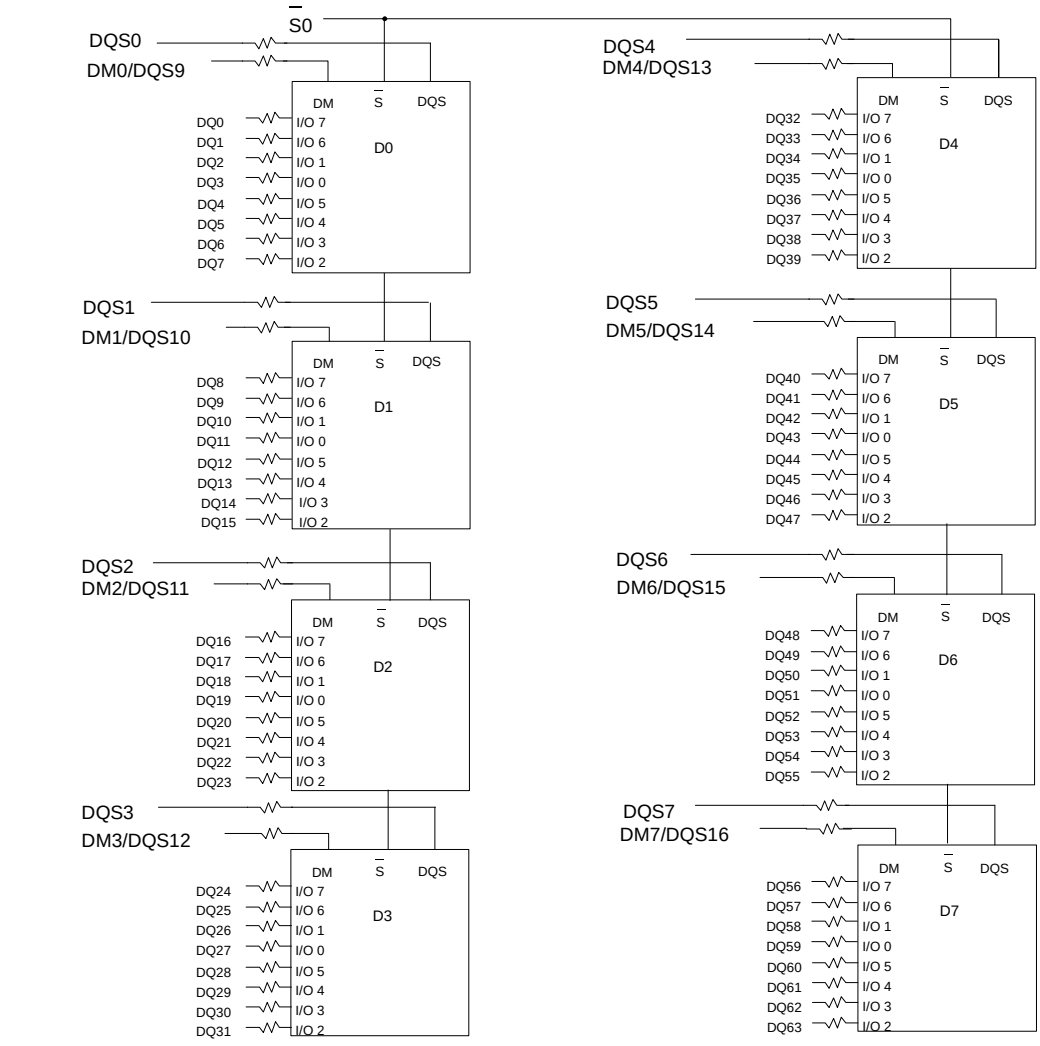


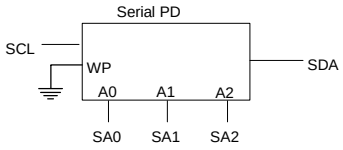
Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms + 5%.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}): STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$ STRAP IN (V_{SS}): V_{DD} p V_{DDQ}.

Block Diagram: Raw Card Version A, x64

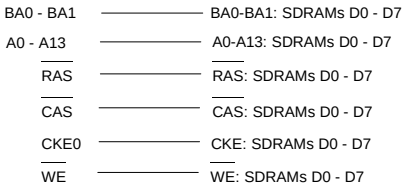
(Populated as 1 physical bank of x8 DDR SDRAMs)

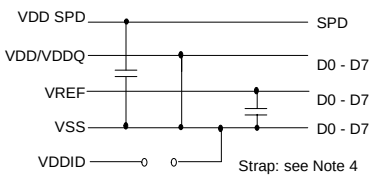




* Clock Wiring	
Clock Input	SDRAMs
*CK0/$\overline{CK0}$	2 SDRAMs
*CK1/$\overline{CK1}$	3 SDRAMs
*CK2/CK2	3 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams



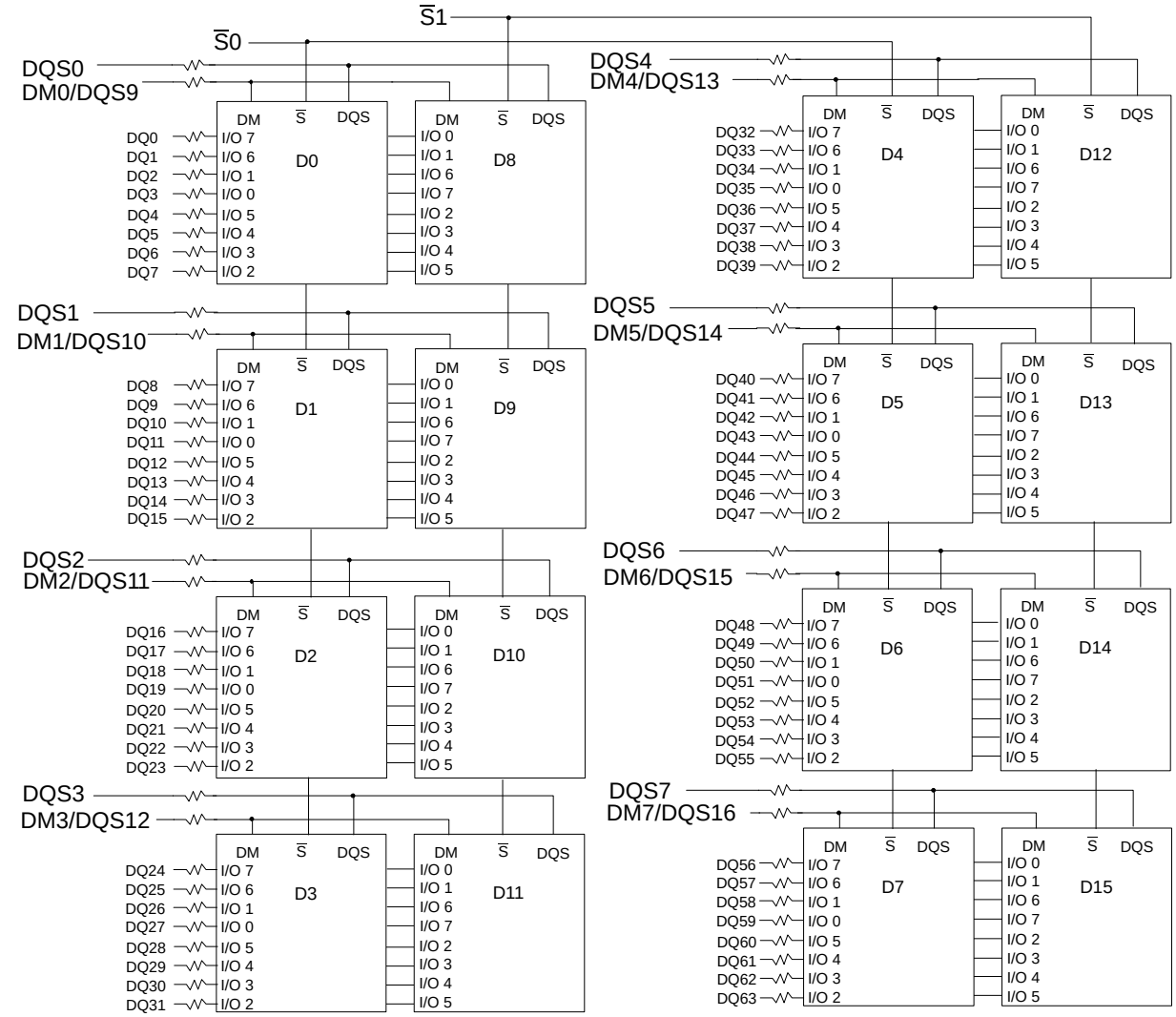


Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms + 5%.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}): STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$ STRAP IN (V_{SS}): V_{DD} p V_{DDQ}.

Block Diagram: Raw Card Version B, x64

(Populated as 2 physical banks of x8 DDR SDRAMs)



BA0 - BA1 — BA0-BA1: SDRAMs D0 - D15
A0 - A13 — A0-A13: SDRAMs D0 - D15
CKE1 — CKE: SDRAMs D8 - D15
$\overline{RAS}$ — $\overline{RAS}$: SDRAMs D0 - D15
$\overline{CAS}$ — $\overline{CAS}$: SDRAMs D0 - D15
CKE0 — CKE: SDRAMs D0 - D7
$\overline{WE}$ — $\overline{WE}$: SDRAMs D0 - D15

* Clock Wiring	
Clock Input	SDRAMs
*CK0/$\overline{CK0}$	4 SDRAMs
*CK1/$\overline{CK1}$	6 SDRAMs
*CK2/$\overline{CK2}$	6 SDRAMs

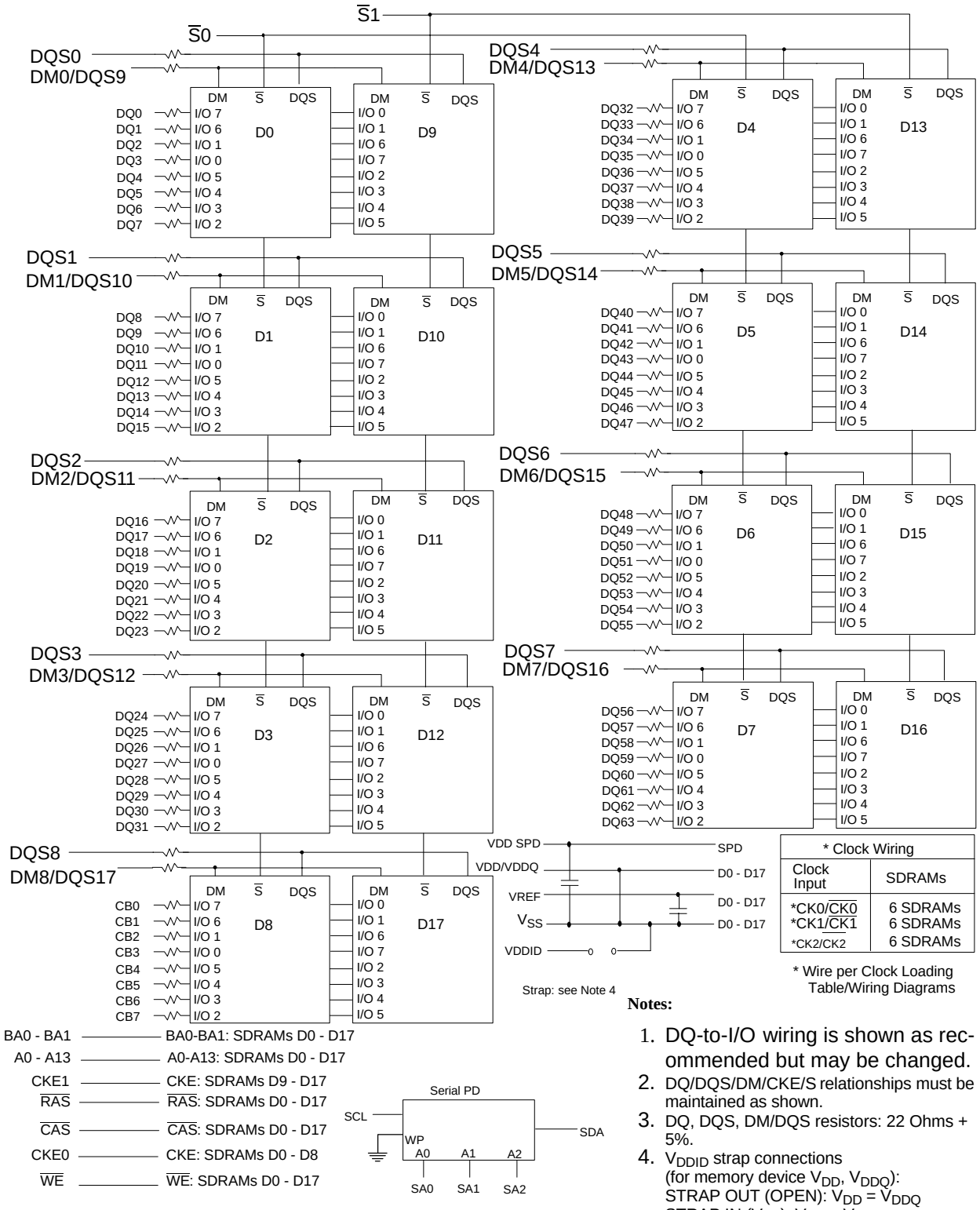
* Wire per Clock Loading Table/Wiring Diagrams

Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms + 5%.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): V_{DD} p V_{DDQ}

Block Diagram: Raw Card Version B, x72

(Populated as 2 physical banks of x8 DDR SDRAMs)



* Clock Wiring	
Clock Input	SDRAMs
*CK0/CK0	6 SDRAMs
*CK1/CK1	6 SDRAMs
*CK2/CK2	6 SDRAMs

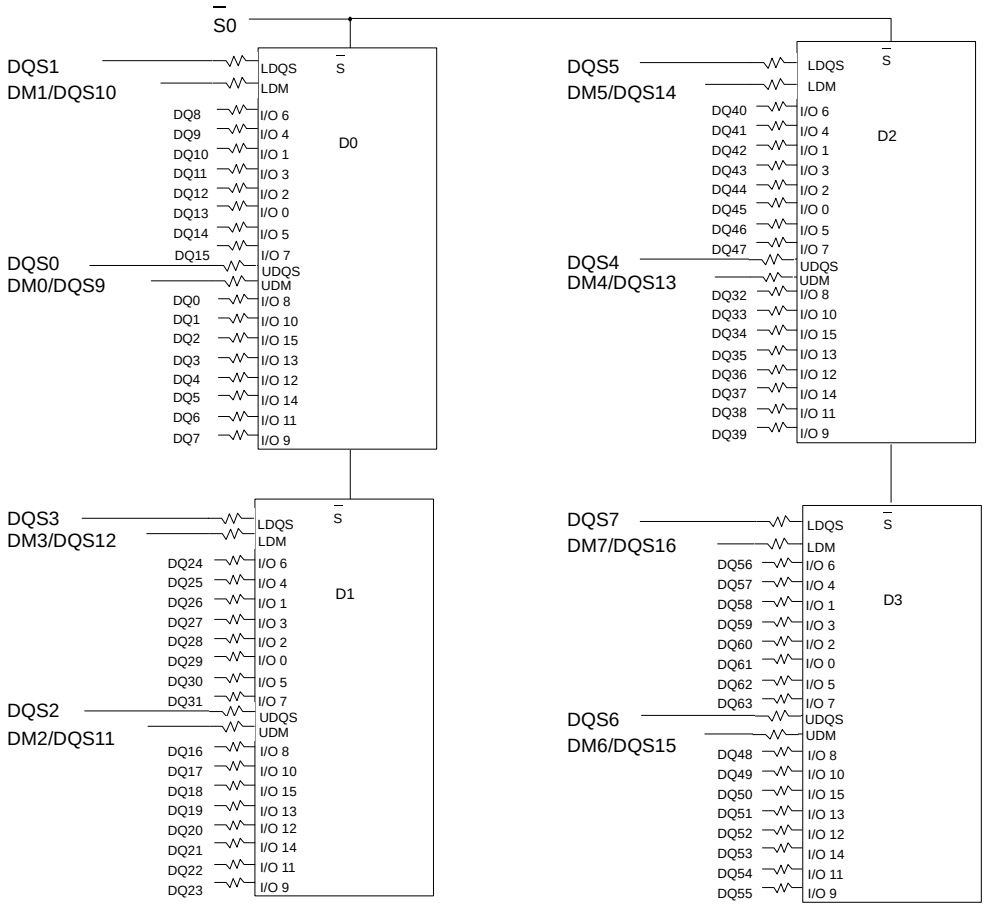
* Wire per Clock Loading Table/Wiring Diagrams

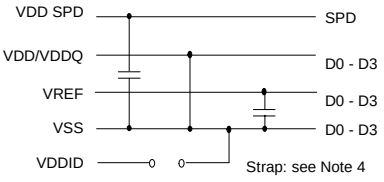
Notes:

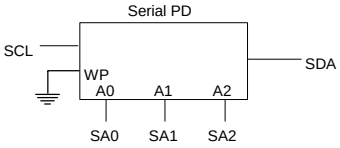
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms + 5%.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): V_{DD} þ V_{DDQ}

Block Diagram: Raw Card Version C, x64

(Populated as 1 physical bank of x16 DDR SDRAMs)

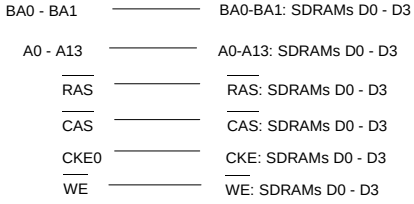






* Clock Wiring	
Clock Input	SDRAMs
*CK0/CK0	NC
*CK1/CK1	2 SDRAMs
*CK2/CK2	2 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams

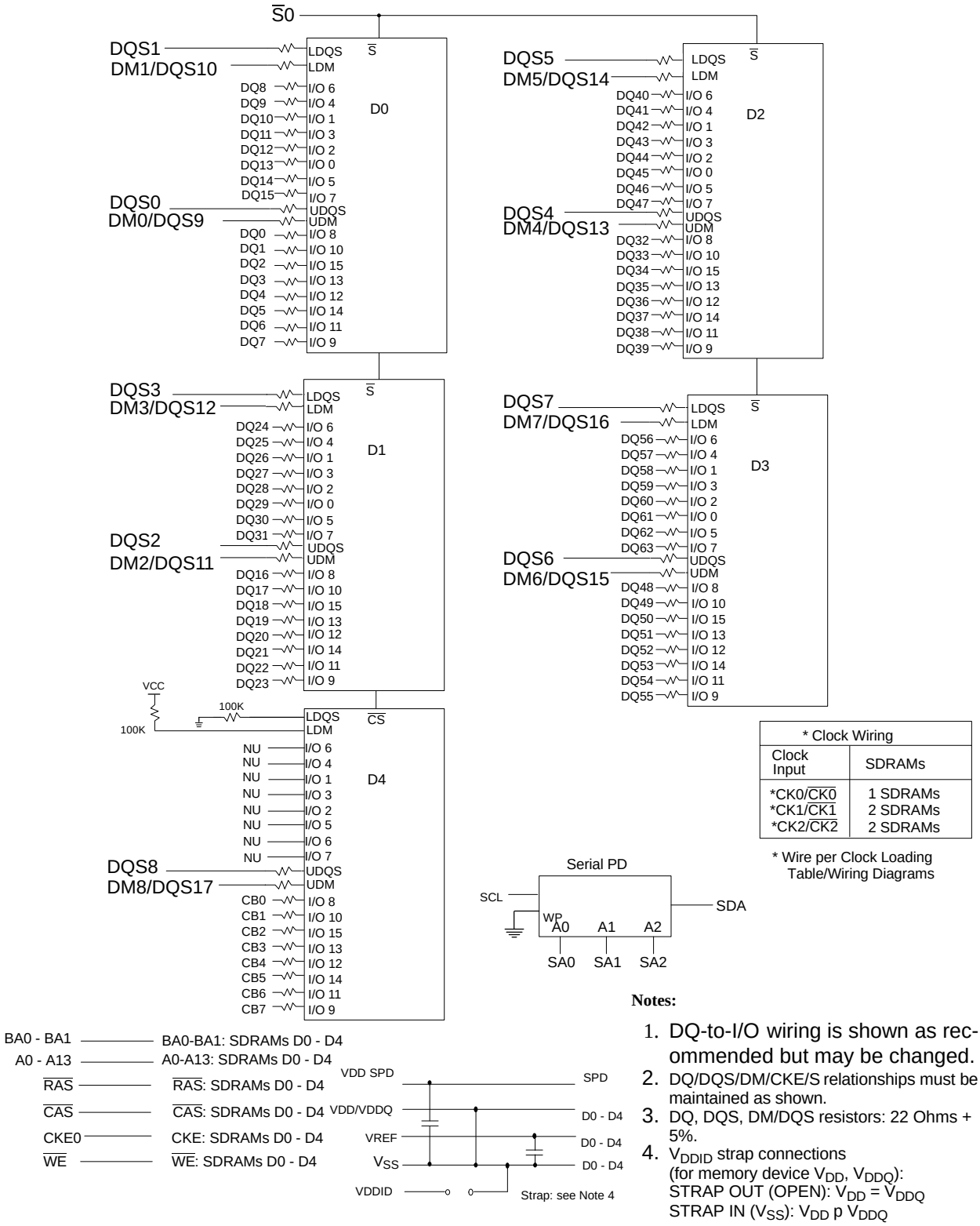


Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms + 5%.
4. V_{DDID} strap connections
   (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): V_{DD} p V_{DDQ}

Block Diagram: Raw Card Version C, x72

(Populated as 1 physical bank of x16 DDR SDRAMs)



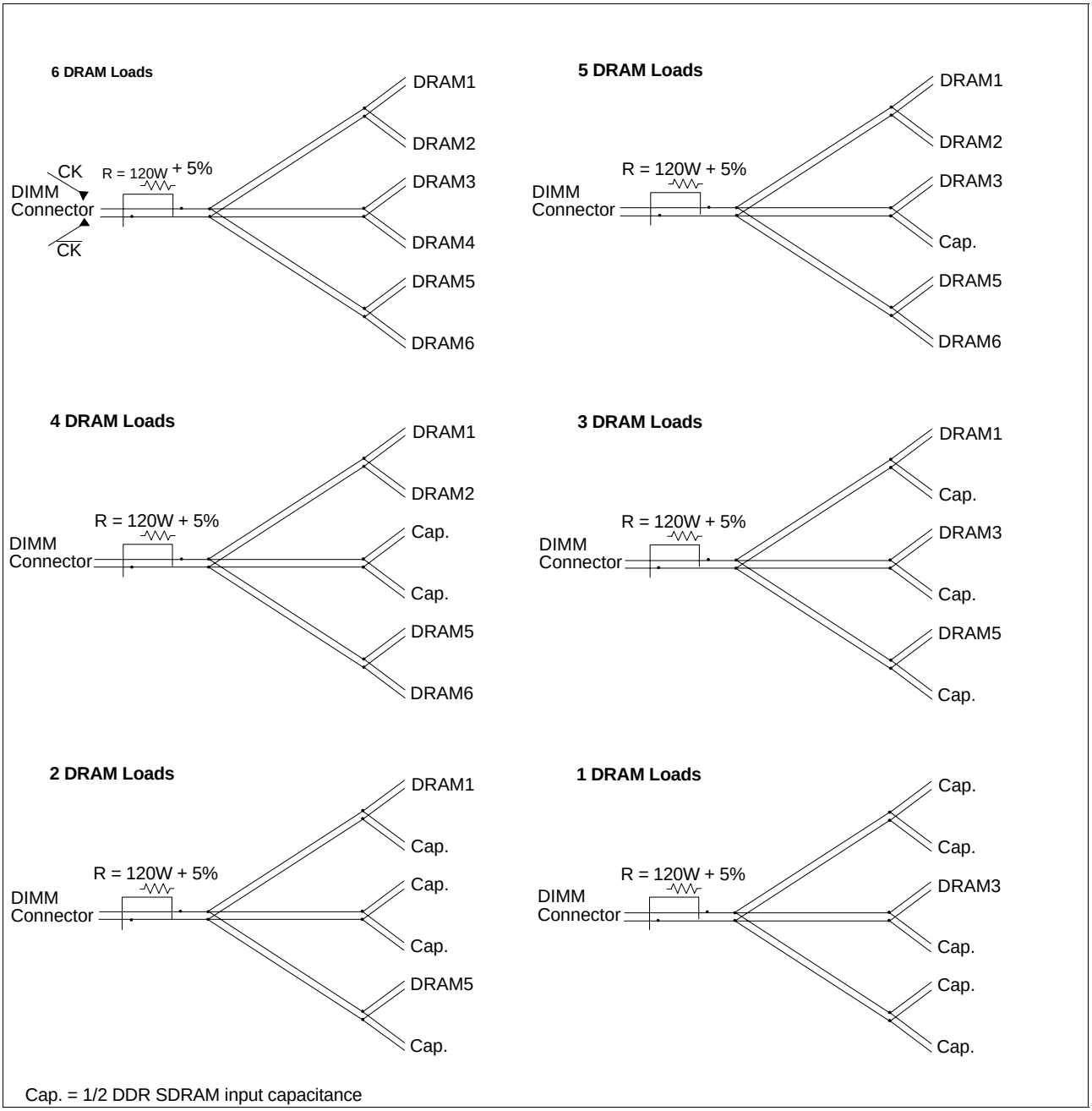
* Clock Wiring	
Clock Input	SDRAMs
*CK0/CK0	1 SDRAMs
*CK1/CK1	2 SDRAMs
*CK2/CK2	2 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams

Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms + 5%.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}): STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$ STRAP IN (V_{SS}): V_{DD} p V_{DDQ}

Logical Clock Net Structures

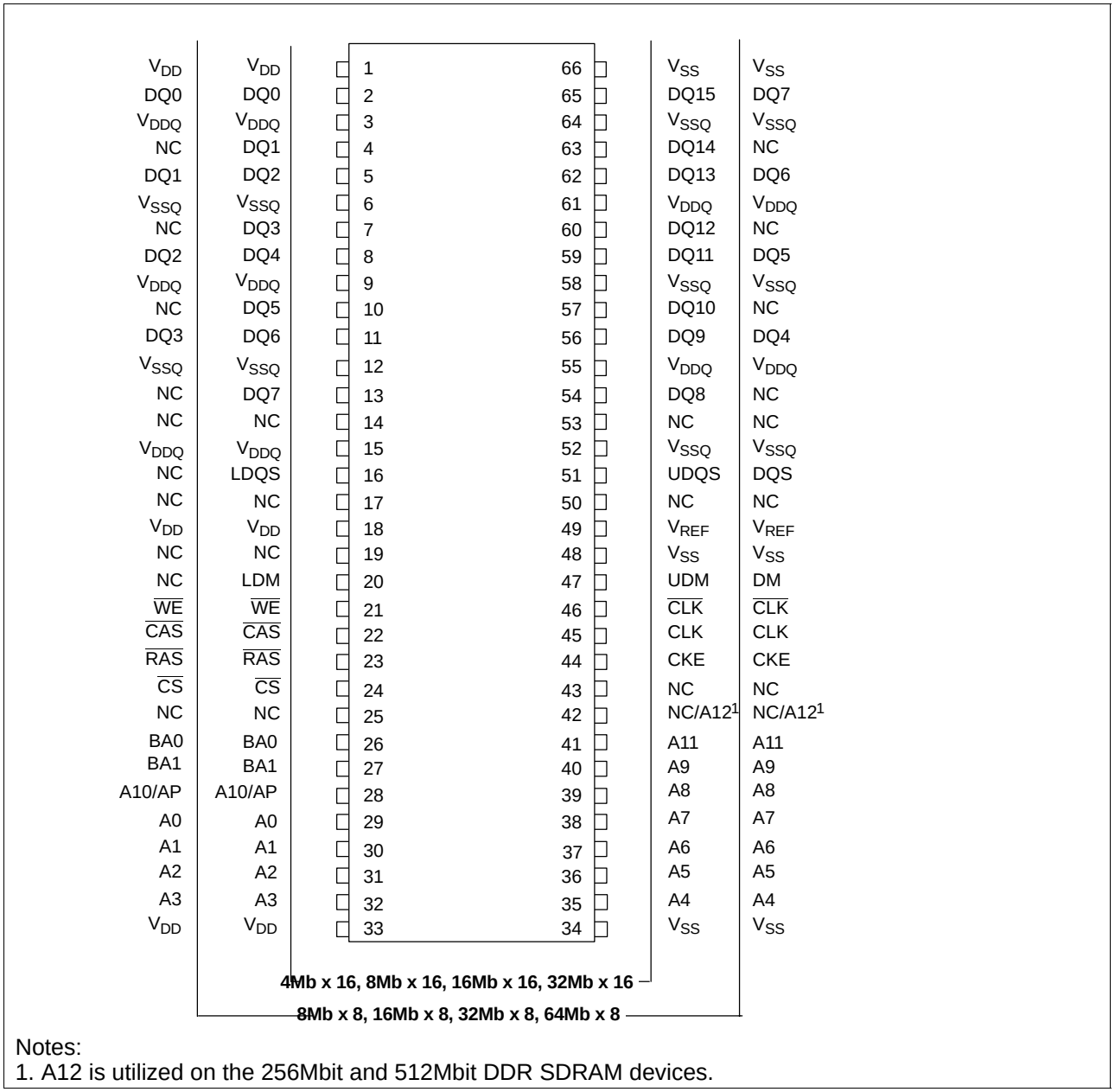


Cap. = 1/2 DDR SDRAM input capacitance

4. Component Details

Pin Assignments for 64Mb, 128Mb, 256Mb and 512Mb DDR SDRAM Planar Components

(Top View)



V_{DD}	V_{DD}	1	66	V_{SS}	V_{SS}
DQ0	DQ0	2	65	DQ15	DQ7
V_{DDQ}	V_{DDQ}	3	64	V_{SSQ}	V_{SSQ}
NC	DQ1	4	63	DQ14	NC
DQ1	DQ2	5	62	DQ13	DQ6
V_{SSQ}	V_{SSQ}	6	61	V_{DDQ}	V_{DDQ}
NC	DQ3	7	60	DQ12	NC
DQ2	DQ4	8	59	DQ11	DQ5
V_{DDQ}	V_{DDQ}	9	58	V_{SSQ}	V_{SSQ}
NC	DQ5	10	57	DQ10	NC
DQ3	DQ6	11	56	DQ9	DQ4
V_{SSQ}	V_{SSQ}	12	55	V_{DDQ}	V_{DDQ}
NC	DQ7	13	54	DQ8	NC
NC	NC	14	53	NC	NC
V_{DDQ}	V_{DDQ}	15	52	V_{SSQ}	V_{SSQ}
NC	LDQS	16	51	UDQS	DQS
NC	NC	17	50	NC	NC
V_{DD}	V_{DD}	18	49	V_{REF}	V_{REF}
NC	NC	19	48	V_{SS}	V_{SS}
NC	LDM	20	47	UDM	DM
$\overline{WE}$	$\overline{WE}$	21	46	$\overline{CLK}$	$\overline{CLK}$
$\overline{CAS}$	$\overline{CAS}$	22	45	CLK	CLK
$\overline{RAS}$	$\overline{RAS}$	23	44	CKE	CKE
$\overline{CS}$	$\overline{CS}$	24	43	NC	NC
NC	NC	25	42	NC/A12[1]	NC/A12[1]
BA0	BA0	26	41	A11	A11
BA1	BA1	27	40	A9	A9
A10/AP	A10/AP	28	39	A8	A8
A0	A0	29	38	A7	A7
A1	A1	30	37	A6	A6
A2	A2	31	36	A5	A5
A3	A3	32	35	A4	A4
V_{DD}	V_{DD}	33	34	V_{SS}	V_{SS}

Notes:
1. A12 is utilized on the 256Mbit and 512Mbit DDR SDRAM devices.

DDR SDRAM Component Specifications

The DDR SDRAM components used with this DIMM design specification are intended to be consistent with JEDEC ballots JC-42.3-98-227A. DDR SDRAM component specification violations also violate the DDR SDRAM Unbuffered DIMM specifications.

5. Unbuffered DIMM Details

SDRAM Module Configurations (Reference Designs)

Raw Card Version	DIMM Capacity	DIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# Address bits row/col
A	64 MB	8Mx64	64Mbit	8Mx8	8	66 lead TSOP	1	4	12/9
		8Mx72	64Mbit	8Mx8	9	66 lead TSOP	1	4	12/9
	128MB	16Mx64	128Mbit	16Mx8	8	66 lead TSOP	1	4	12/10
		16Mx72	128Mbit	16Mx8	9	66 lead TSOP	1	4	12/10
	256MB	32Mx64	256Mbit	32Mx8	8	66 lead TSOP	1	4	13/10
		32Mx72	256Mbit	32Mx8	9	66 lead TSOP	1	4	13/10
	512MB	64Mx64	512Mbit	64Mx8	8	66 lead TSOP	1	4	13/11
		64Mx72	512Mbit	64Mx8	9	66 lead TSOP	1	4	13/11
B	128MB	16Mx64	64Mbit	8Mx8	16	66 lead TSOP	2	4	12/10
		16Mx72	64Mbit	8Mx8	18	66 lead TSOP	2	4	12/10
	256MB	32Mx64	128Mbit	16Mx8	16	66 lead TSOP	2	4	12/10
		32Mx72	128Mbit	16Mx8	18	66 lead TSOP	2	4	12/10
	512MB	64Mx64	256Mbit	32Mx8	16	66 lead TSOP	2	4	13/10
		64Mx72	256Mbit	32Mx8	18	66 lead TSOP	2	4	13/10
	1GB	128Mx64	512Mbit	64Mx8	16	66 lead TSOP	2	4	13/11
		128Mx72	512Mbit	64Mx8	18	66 lead TSOP	2	4	13/11
C	32MB	4Mx64	64Mbit	4Mx16	4	66 lead TSOP	1	4	12/8
		4Mx72	64Mbit	4Mx16	5	66 lead TSOP	1	4	12/8
	64MB	8Mx64	128Mbit	8Mx16	4	66 lead TSOP	1	4	12/9
		8Mx72	128Mbit	8Mx16	5	66 lead TSOP	1	4	12/9
	128MB	16Mx64	256Mbit	16Mx16	4	66 lead TSOP	1	4	12/10
		16Mx72	256Mbit	16Mx16	5	66 lead TSOP	1	4	12/10
	256MB	32Mx64	512Mbit	32Mx16	4	66 lead TSOP	1	4	13/10
		32Mx72	512Mbit	32Mx16	5	66 lead TSOP	1	4	13/10

Input Loading Matrix

Signal Names	Input Device	R/C A	R/C B	R/C C
Clock (CK0 - CK2)	SDRAM[1]	6	6	6
CKE0/CKE1/Chipselects	SDRAM	8-9	8-9	4-5
Addr/RAS/CAS/BA/WE	SDRAM	8-9	16-18	4-5
DQ/CB/DQS/DM	SDRAM	1	2	1
SCL/SDA/SA	EEPROM	1	1	1
1. 6 SDRAMs or equivalent using padding capacitors				

DDR Unbuffered Design File Releases

'Reference' design file updates will be released as needed. This DDR Unbuffered DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated. The following table outlines the most recent design file releases.

Note: Future design file releases will include both a date and a revision label. All changes to the design file are also documented within the 'read-me' file.

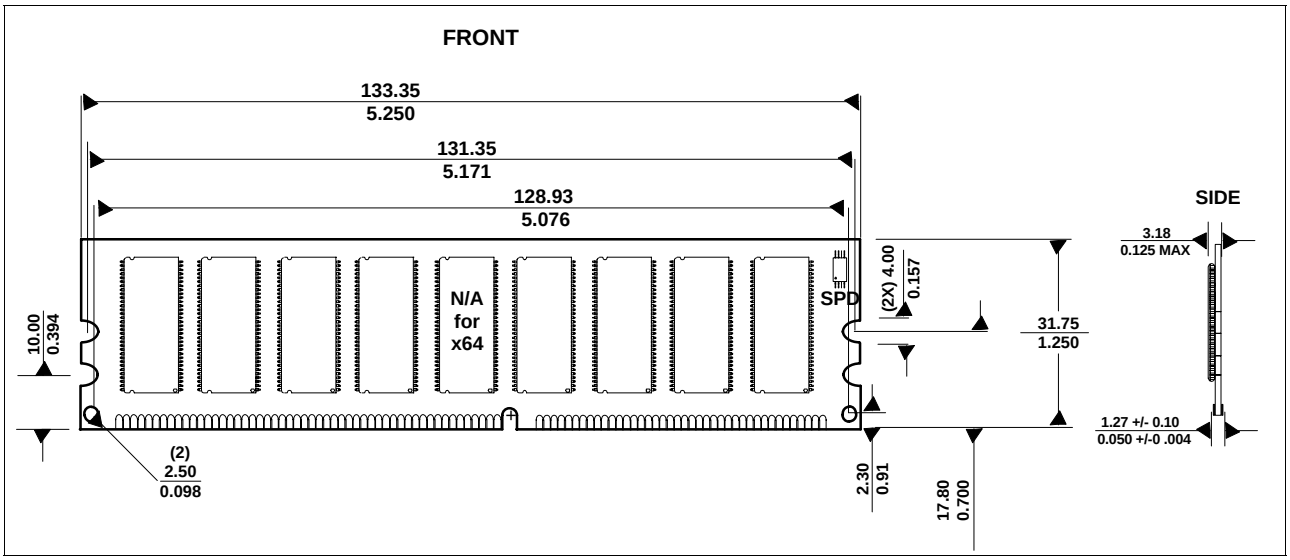
Raw Card Version	Specification Revision	Applicable Gerber File	Notes
A	0.9	A0	A1 Release Target: 05/31/00
B	0.9	B1	Production ready
C	0.9	C1	Production ready

Component Types and Placement

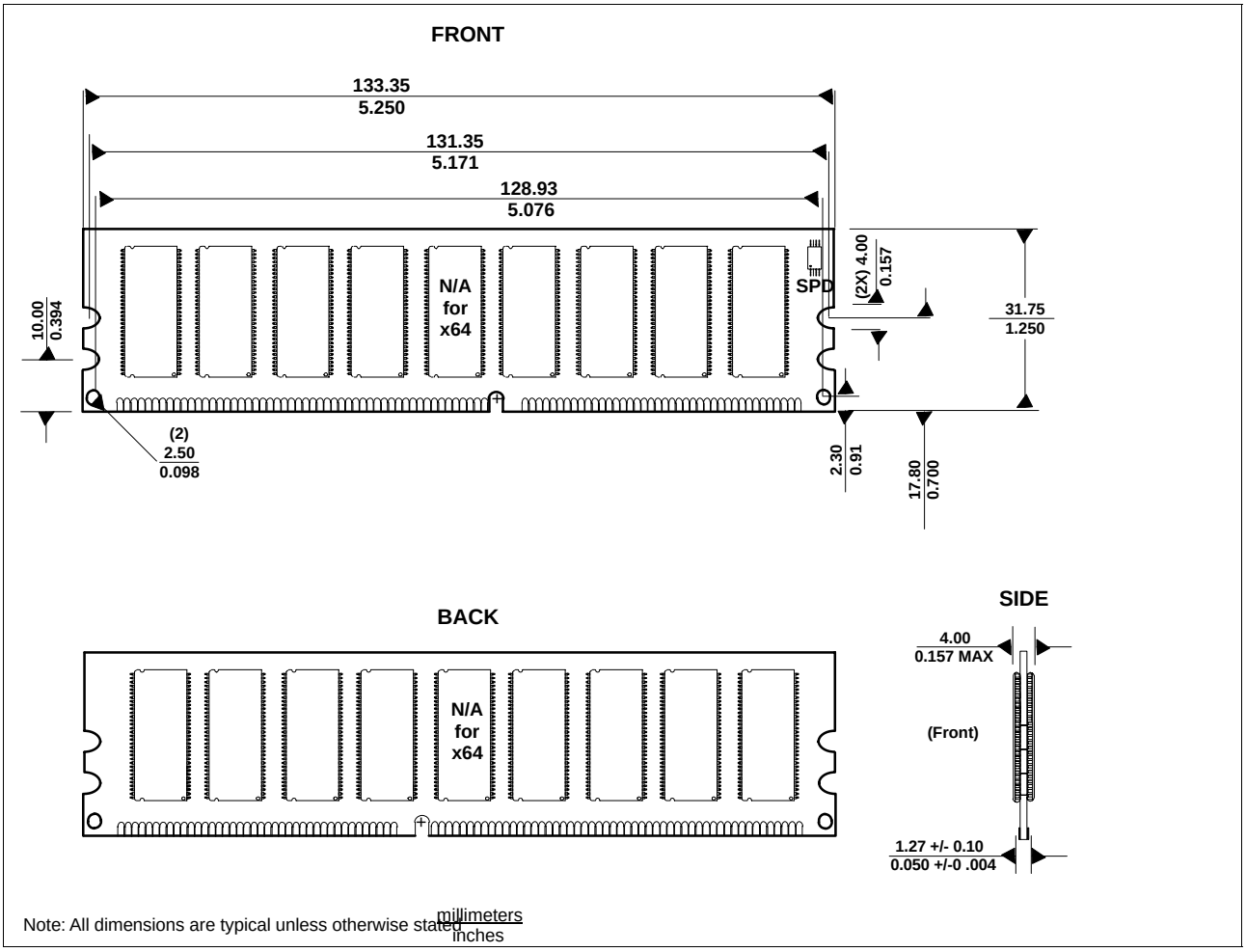
Components shall be positioned on the PCB to meet the minimum and maximum trace lengths required for DDR SDRAM signals. Bypass capacitors for DDR SDRAM devices must be located near the device power pins.

The following layouts suggest placement for the Raw Card Versions A, B and C. Exact spacing is not provided, but should be based on manufacturing contraints and signal routing constraints imposed by this design guide.

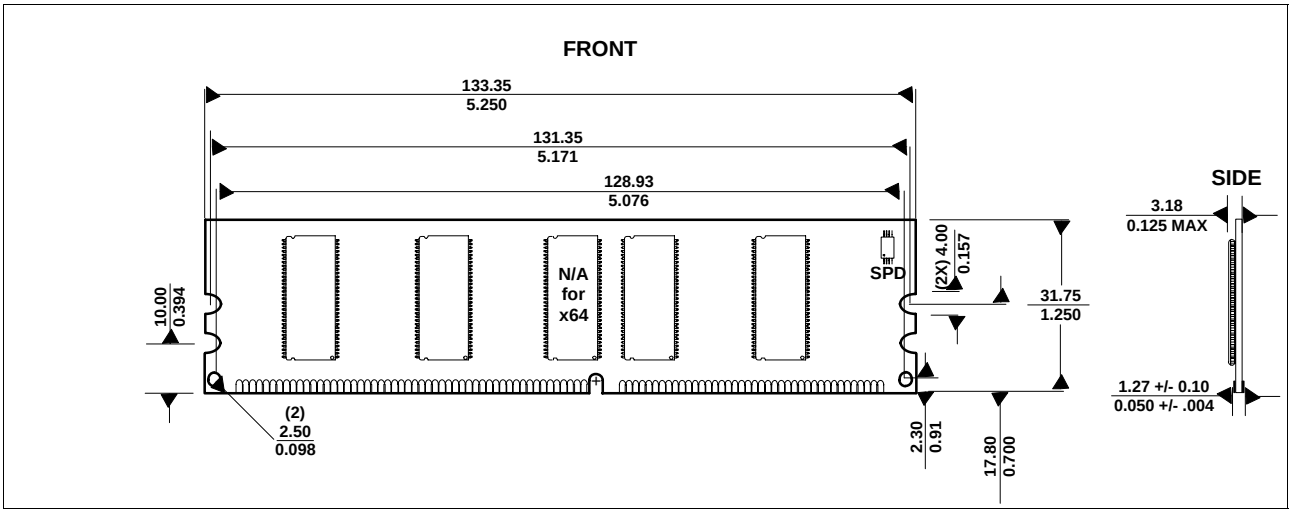
Example Raw Card A Component Placement



Example Raw Card B Component Placement



Example Raw Card C Component Placement



6. DIMM Wiring Details

Signal Groups

This specification categorizes DDR SDRAM timing-critical signals into five groups. The following table summarizes the signals contained in each group.

Signal Group	Signals In Group	Raw Card Version	Page
Clock	CK [3:0]	A, B, C	23
Data	DQ [63:0]; CB [7:0]; DQS [8:0], DM [8:0]	A, B, C	24
Chip Select	S [0,1]	A, B	26
	S [0,1]	C	27
Clock Enable	CKE [0,1]	A, B	27
	CKE [0,1]	C	30
Address/Control	Ax, BAx, RAS, CAS, WE	A,B	29
	Ax, BAx, RAS, CAS, WE	C	33

General Net Structure Routing Guidelines

Net structures and lengths must satisfy signal quality and setup/hold time requirements for the memory interface. Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace length table that lists the minimum and maximum allowable lengths for each trace segment and/or net.

The general routing requirements are as follows

- Route all signal traces including differential clocks using 4/6 rules, i.e., 4 mil traces and 6 mil minimum spacing between adjacent traces.
- No test points are required.

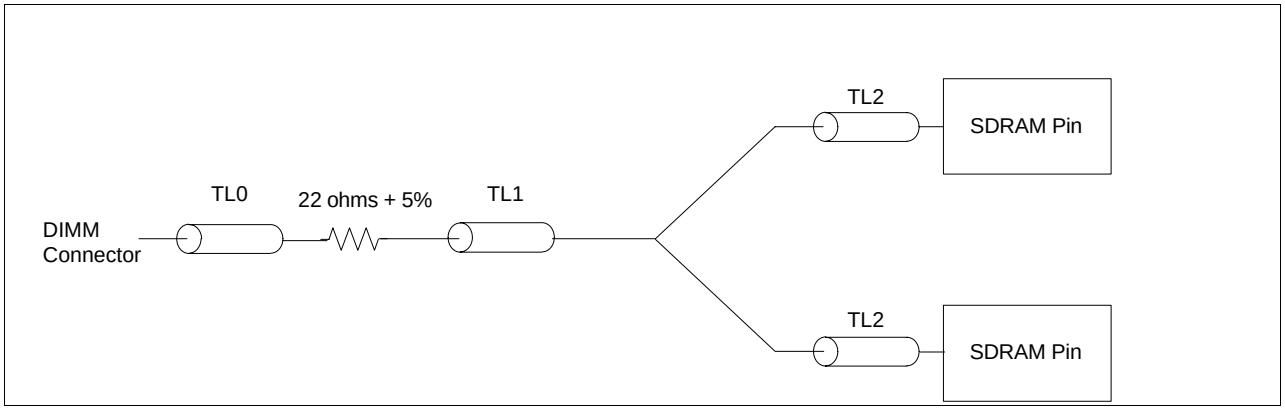
Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for registered DIMM designs. The diagrams should be used to determine individual signal wiring on a DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify DIMM functionality, a full simulation of all signal integrity and timing is required. The given net structures and trace lengths are not inclusive for all solutions.

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input. The net structure routing description in this document represents the planned net structures for Raw Card Versions A, B and C. Complete net structures will be added in future revsions upon DIMM design completion and verification.

Net Structure Example

A 128MB double-sided ECC DIMM using 64Mbit 8Mx8 DDR SDRAM devices would have a data net structure as shown in the following diagram.



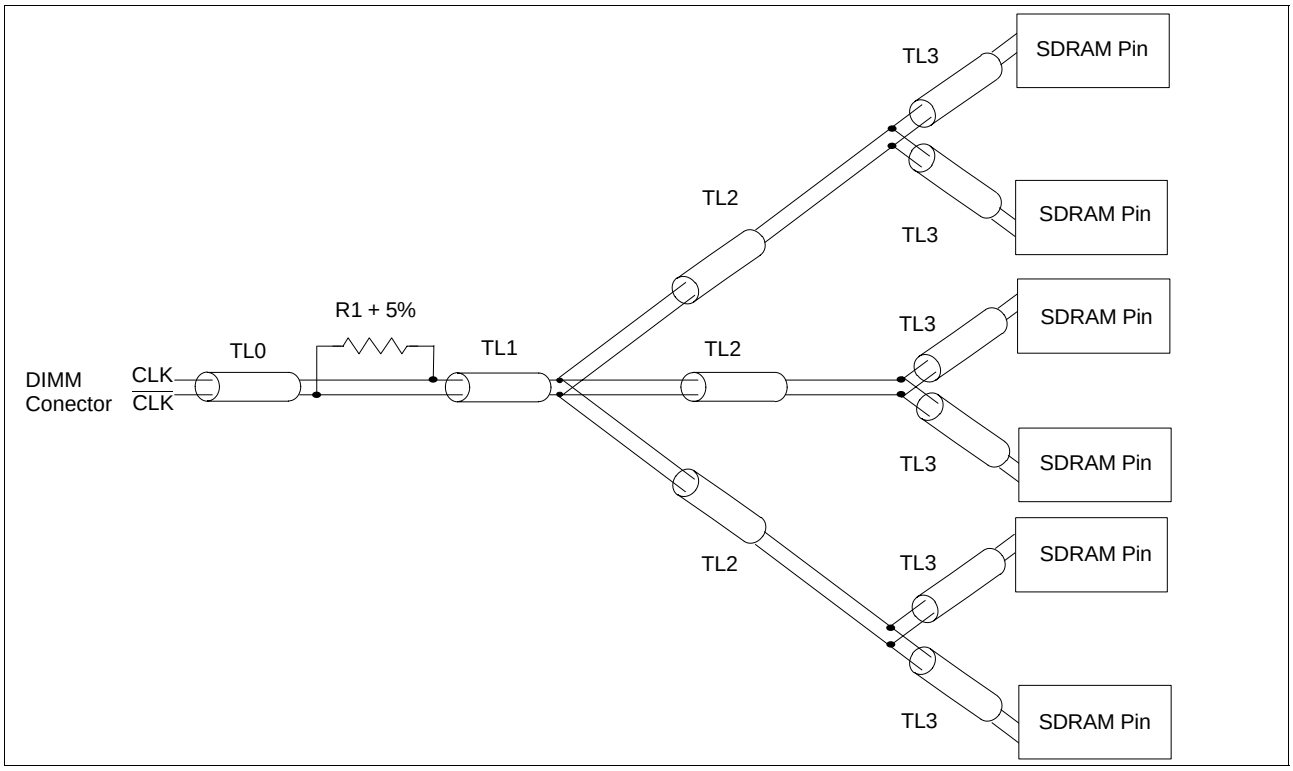
Clock Net Structures

CK[3:0]

SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality
- Rise/fall time
- SDRAM component edge skew
- Motherboard chipset clock edge skew

Net Structure Routing for Clocks



Trace Lengths for Clock Net Structures

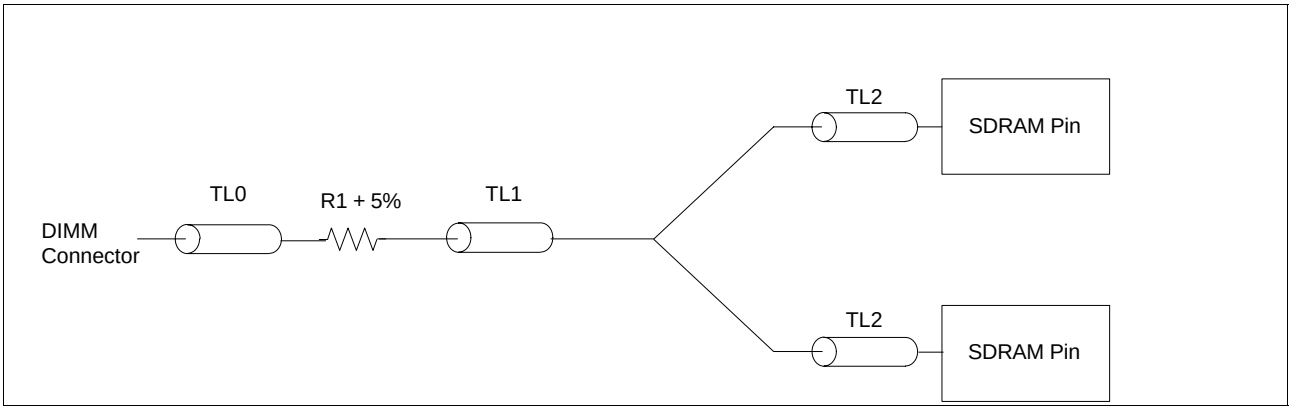
Raw Card	TL0		TL1		TL2		TL3		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max		
A,B	.15	.16	.04	.05	1.13	1.14	.36	.37	120	1,2
C	.15	.16	.04	.05	1.13	1.14	.36	.37	120	1,2

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch
2. Logical clock structures on page 15 must be followed. In some cases the loads will be equivalent capacitors.

Data Net Structures

DQ[63:0], CB[7:0], DQS [8:0] and DM [8:0]

Net Structure Routing for Data (Raw Card Versions A, B and C)



Trace Lengths for DQ, CB and DQS Net Structures

Raw Card	TL0		TL1		TL2		Total		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max		
A, B	.14	.24	.19	.43	.13	.37	.72	.73	22	1,2
C	.14	.16	.57	.58	NA	NA	.72	.73	22	1,2

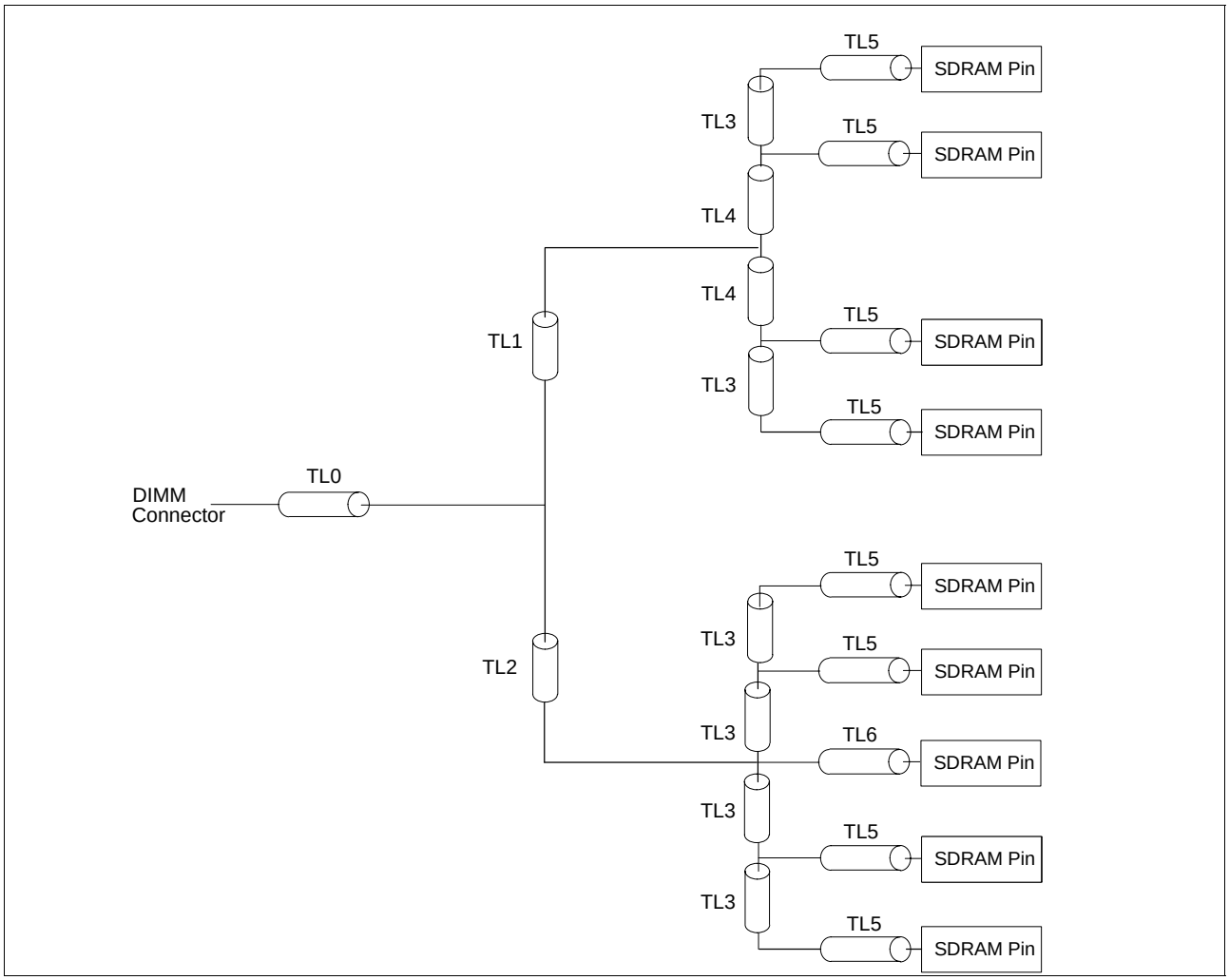
1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch
2. Total Min and Total Max refer to the min and max respectively of TL0 + TL1 + TL2.

Trace Lengths for DM Net Structures

Raw Card	TL0		TL1		TL2		Total		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max		
A, B	.15	.17	.25	.28	.42	.43	.82	.86	22	1,2
C	.14	.15	.68	.69	NA	NA	.83	.84	22	1,2

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch
2. Total Min and Total Max refer to the min and max respectively of TL0 + TL1 + TL2.

Net Structure Routing for Chip Select (Raw Card Version A)

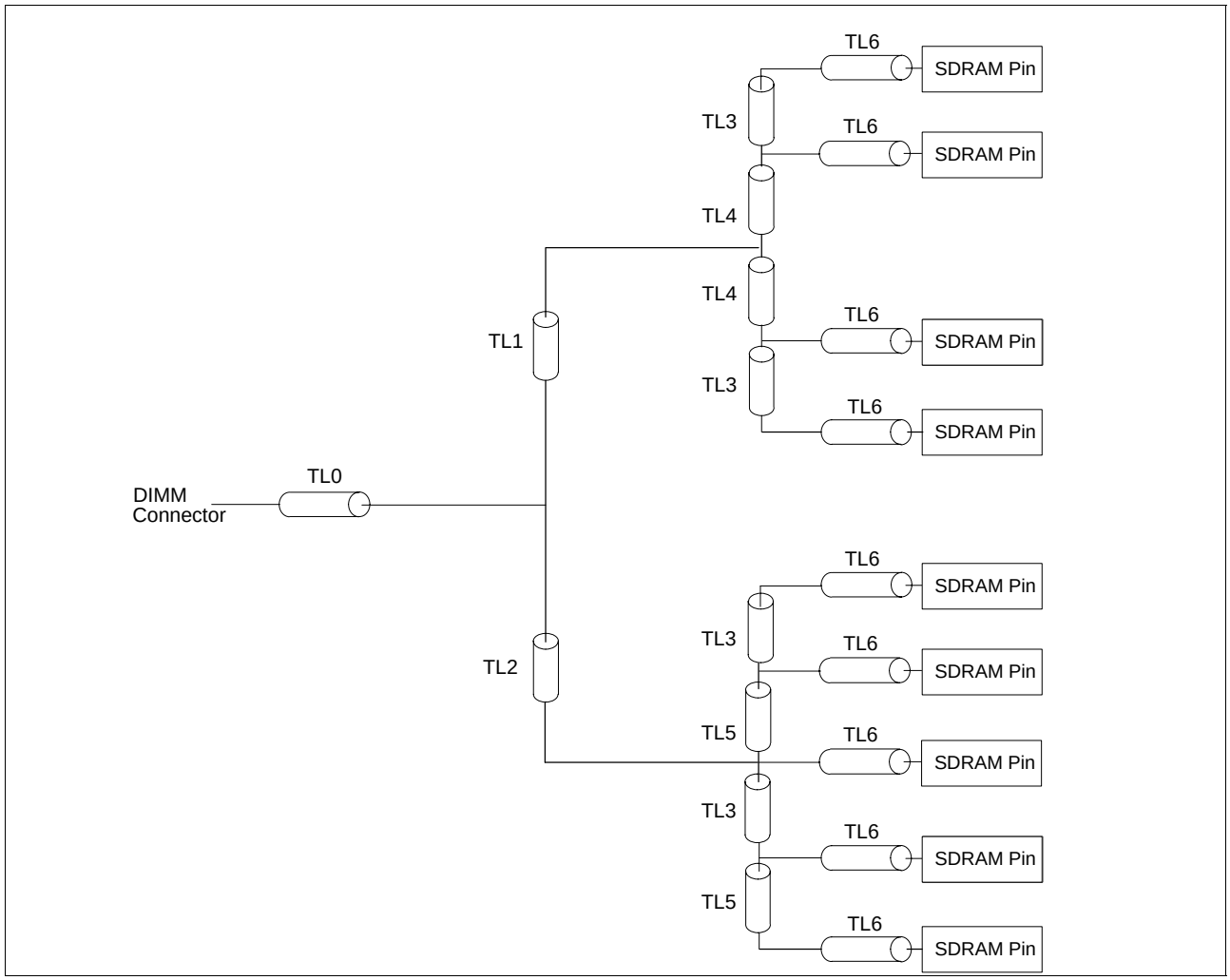


Trace Lengths for Chip Select Net Structures ($\overline{S0}$, $\overline{S1}$)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
A	2.41	2.42	1.57	1.58	1.26	1.27	.58	.60	.29	.30	.15	.16	.32	.33	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Net Structure Routing for Chip Select (Raw Card Version B)

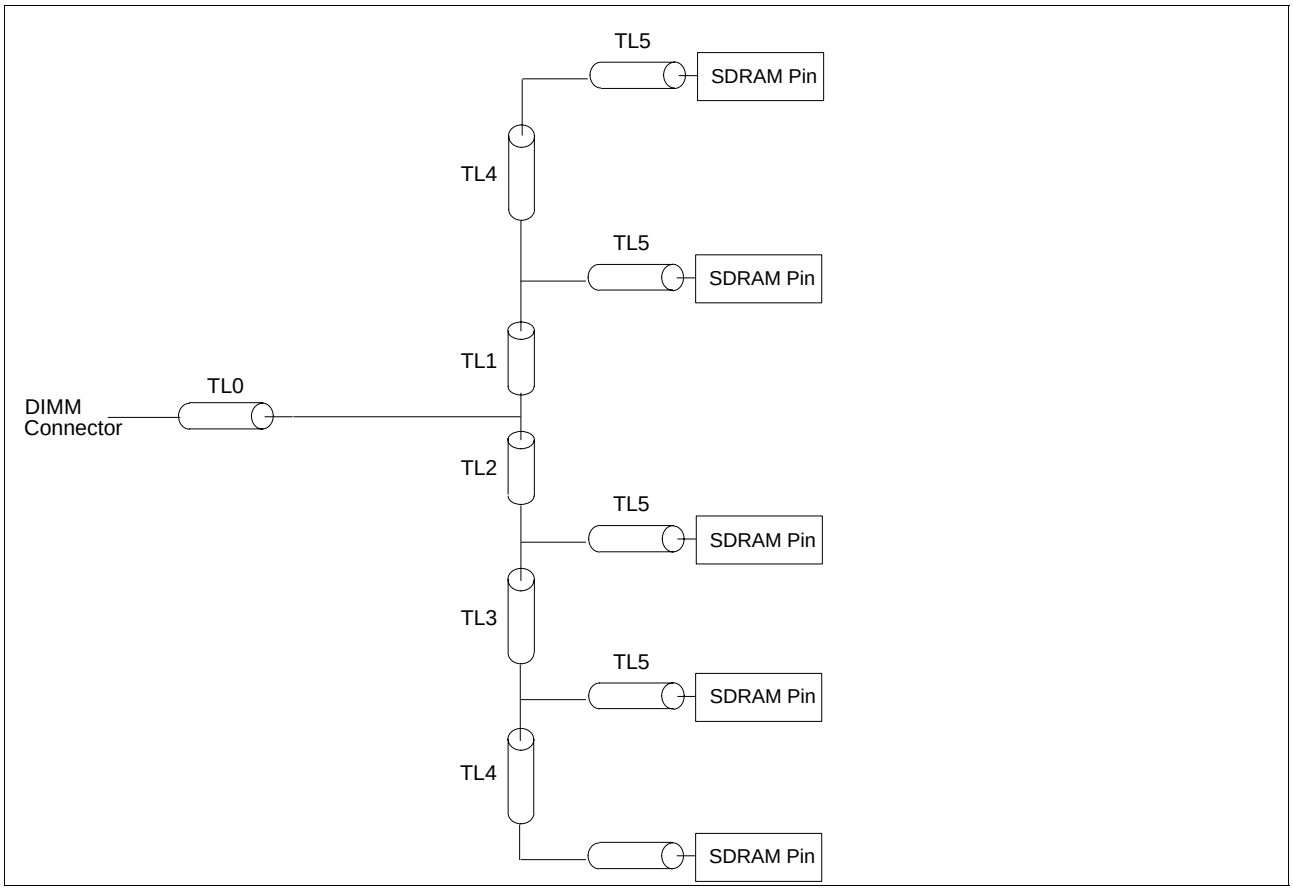


Trace Lengths for Chip Select Net Structures ($\overline{S0}$, $\overline{S1}$)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
B	2.07	2.08	1.76	1.77	1.41	1.42	.41	.59	.34	.35	.67	.75	.13	.35	1,2

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.
2. SDRAMs shown alternate between the front and back of the DIMM.

Net Structure Routing for Chip Select (Raw Card Version C)

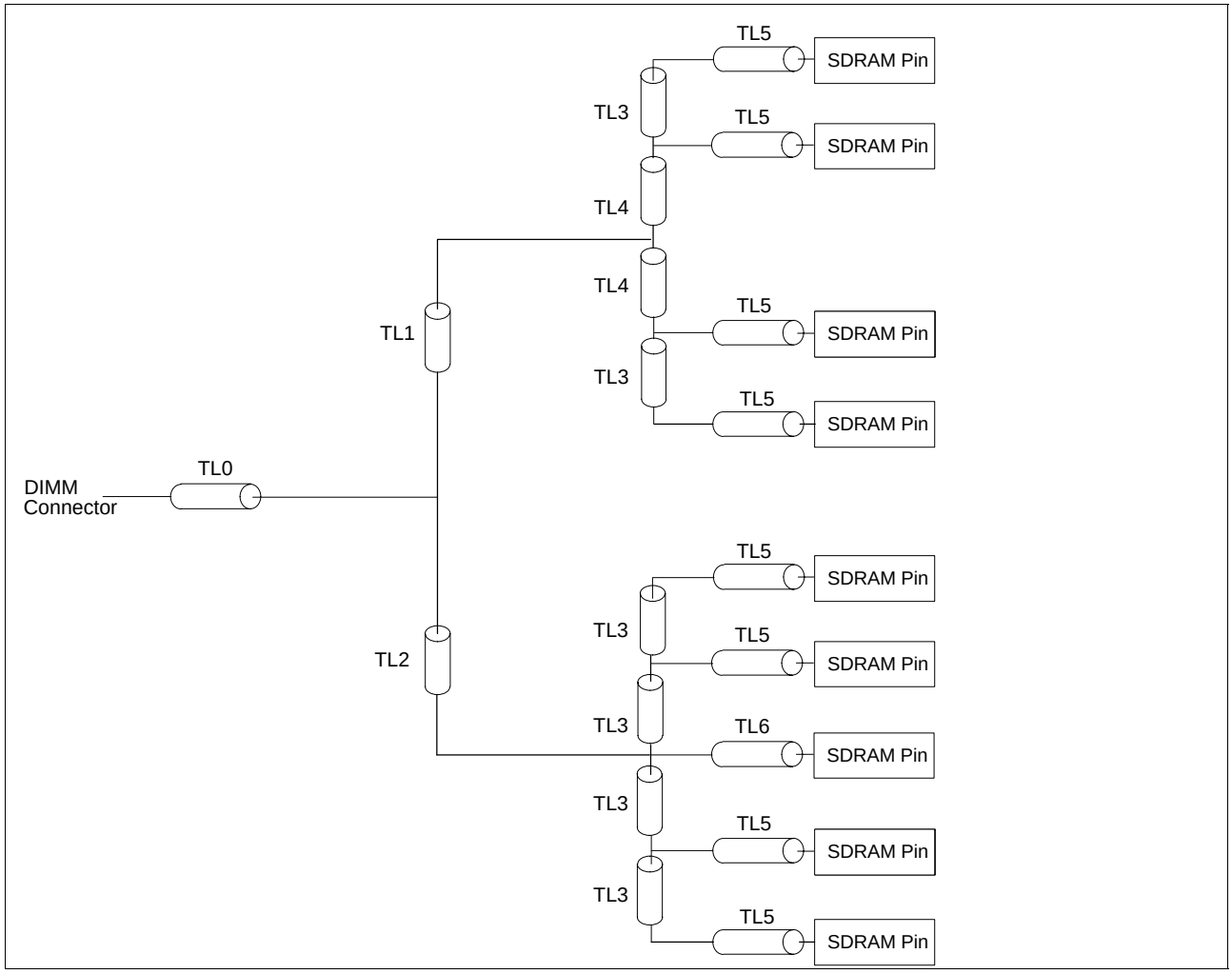


Trace Lengths for Chip Select Net Structures ($\overline{S0}$)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
C	5.70	5.71	.91	.92	.29	.30	.62	.63	.84	.85	.08	.12	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Net Structure Routing for Clock Enable (Raw Card Version A)

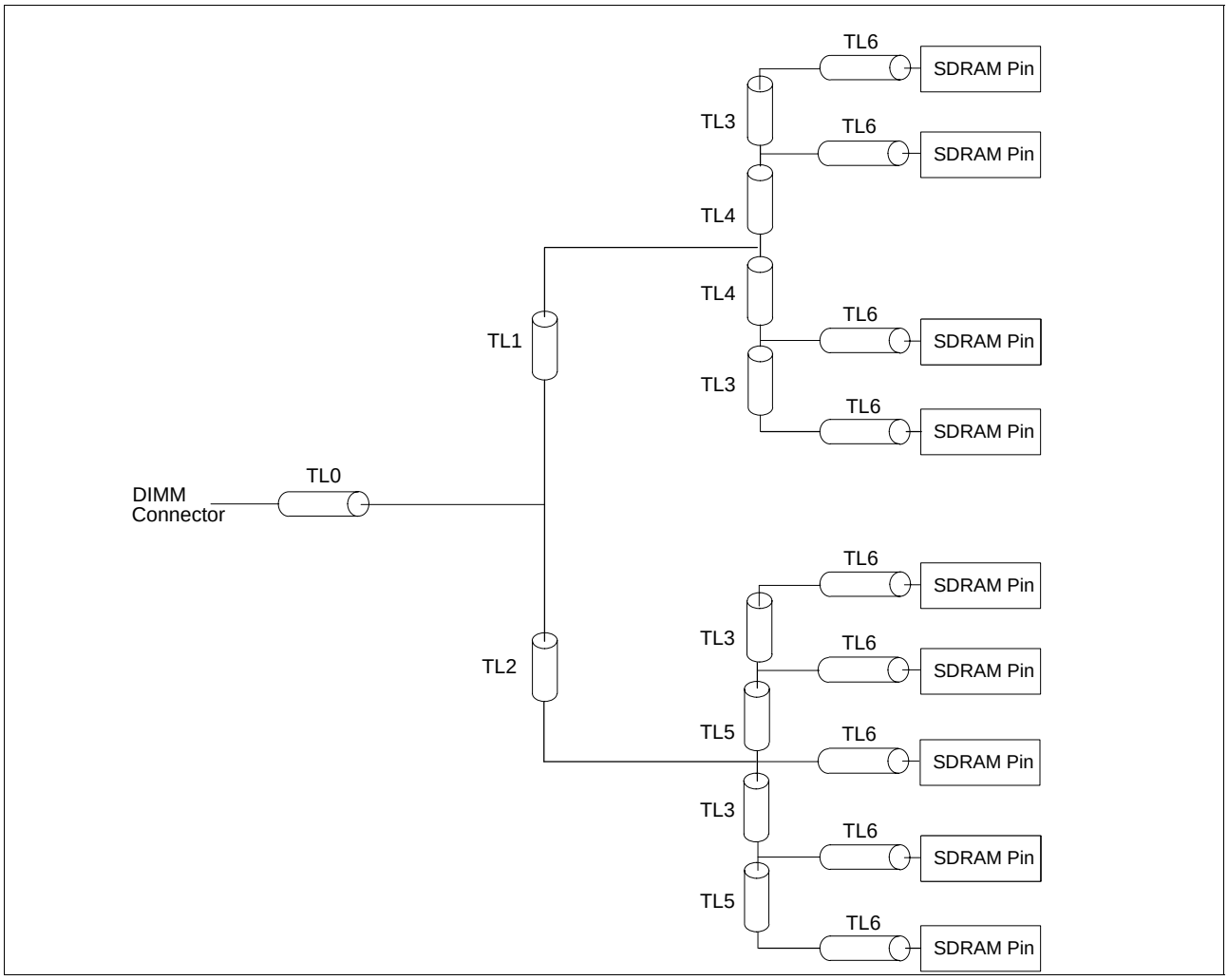


Trace Lengths for Clock Enable Net Structures (CKE0, CKE1)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
A	2.40	2.41	1.57	1.58	1.26	1.27	.57	.58	.30	.31	.16	.17	.32	.33	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Net Structure Routing for Clock Enable (Raw Card Version B)

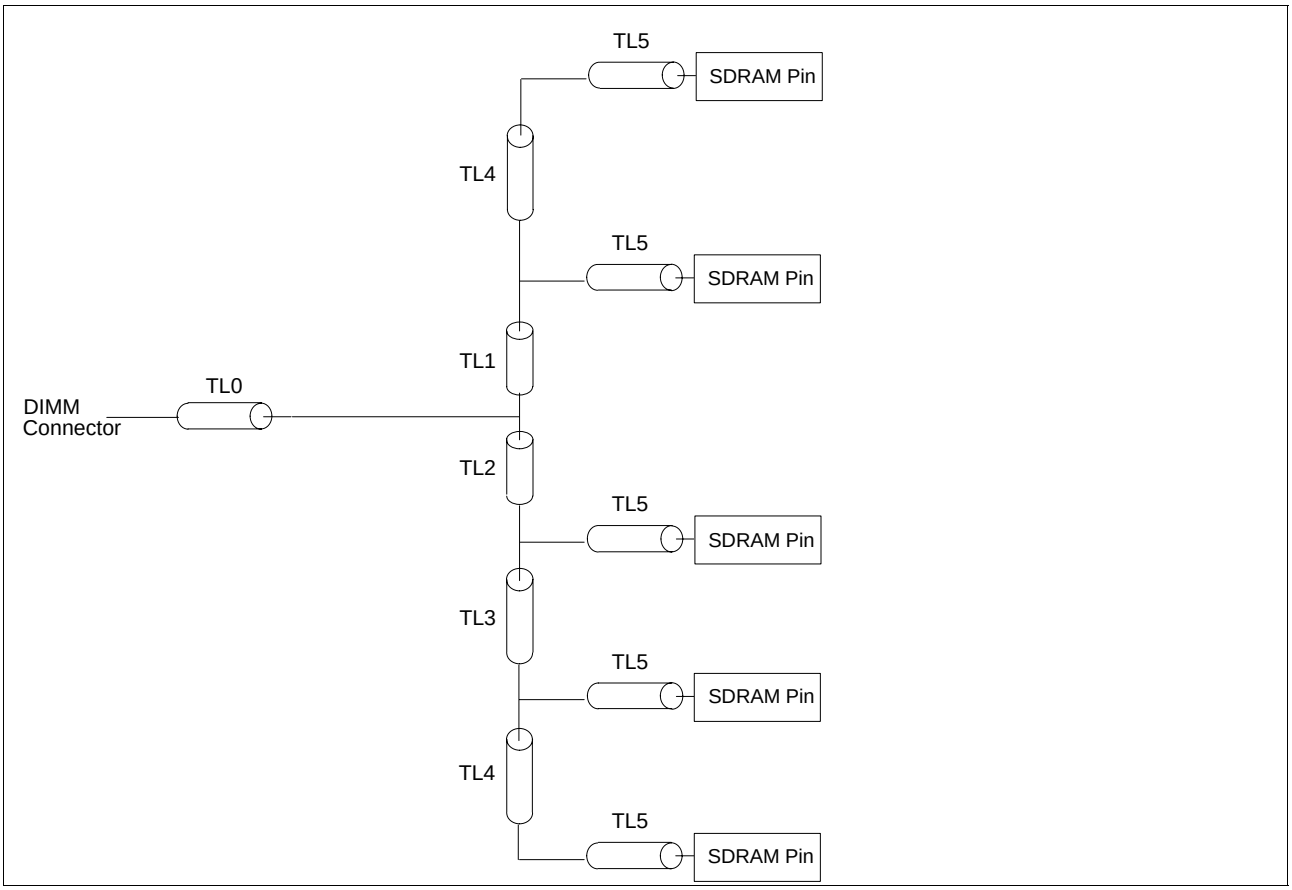


Trace Lengths for Clock Enable Net Structures (CKE0, CKE1)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
B	2.45	2.46	1.55	1.56	1.24	1.25	.44	.57	.41	.44	.55	.70	.22	.33	1,2

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.
2. SDRAMs shown alternate between the front and back of the DIMM.

Net Structure Routing for Clock Enable (Raw Cards Version C)



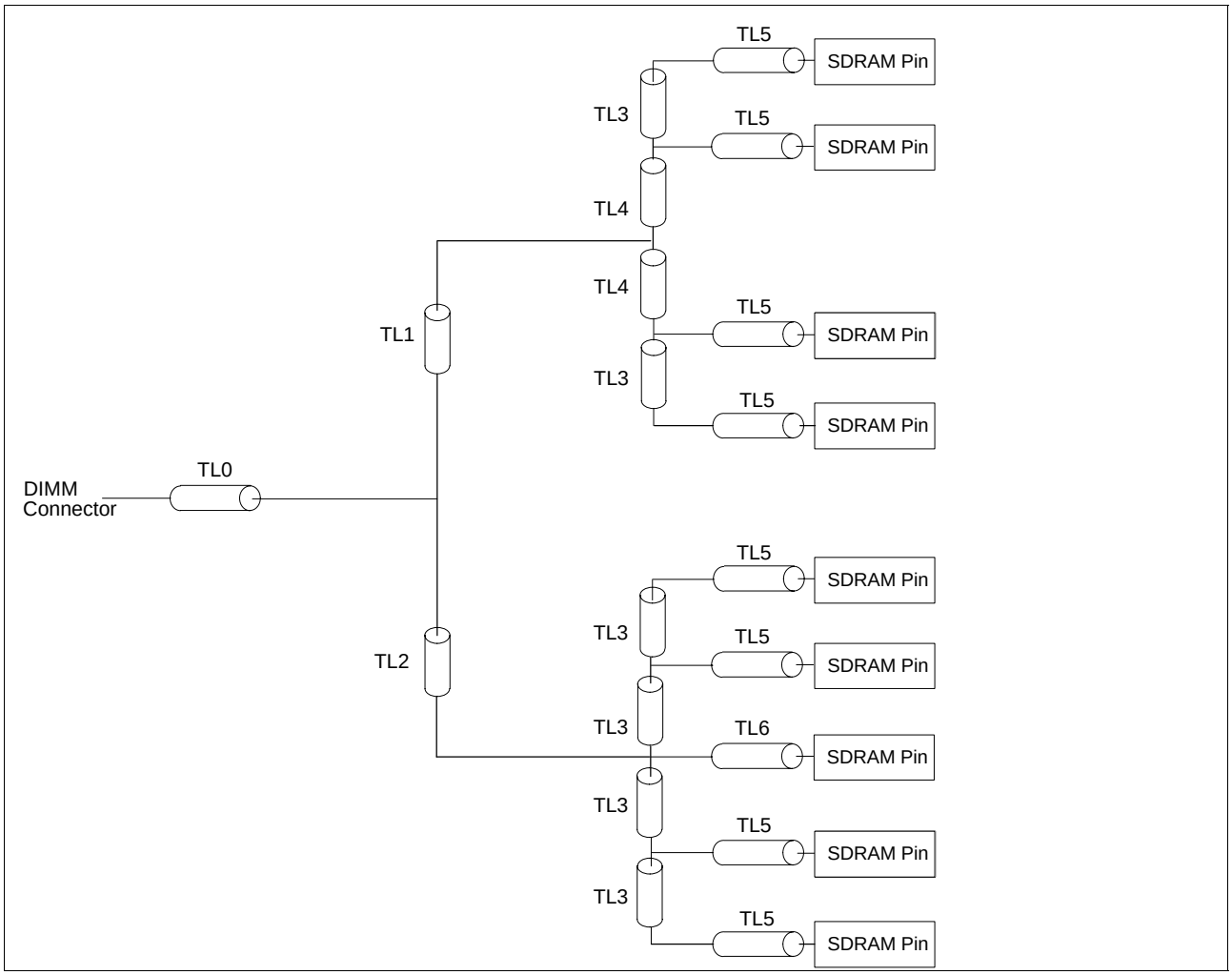
Trace Lengths for Clock Enable Net Structures (CKE0)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
C	5.66	5.67	.91	.92	.29	.30	.62	.63	.84	.85	.08	.12	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Net Structure Routing for Address and Control (Raw Card Version A)

A, BA, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ for Raw Card Version A

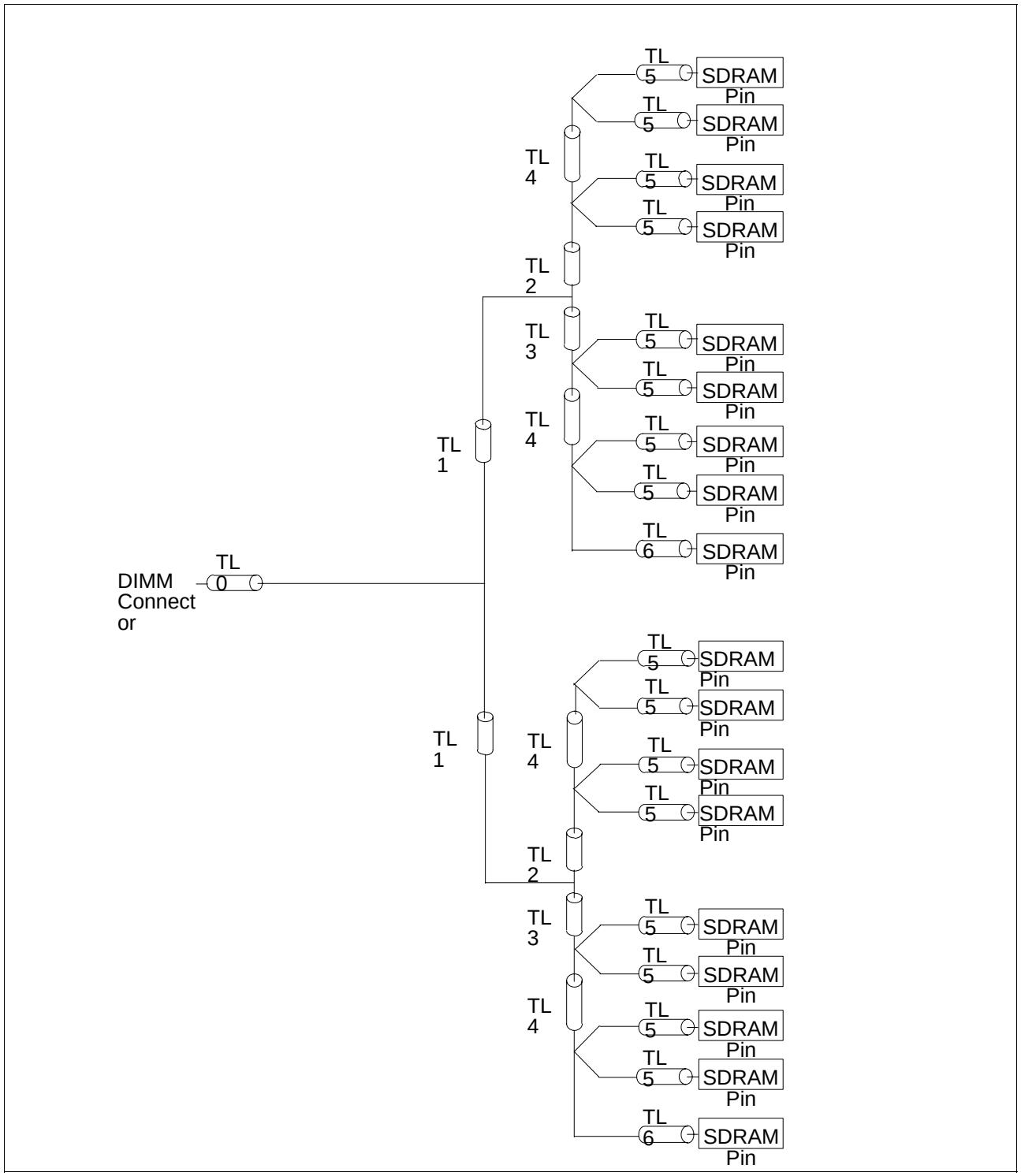


Trace Lengths for Address and Control Net Structures

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
A	2.36	2.77	1.54	1.67	1.23	1.34	.54	.60	.30	.33	.14	.18	.32	.33	1
1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.															

Net Structure Routing for Address and Control (Raw Card Version B)

A, BA, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ for Raw Card Version B



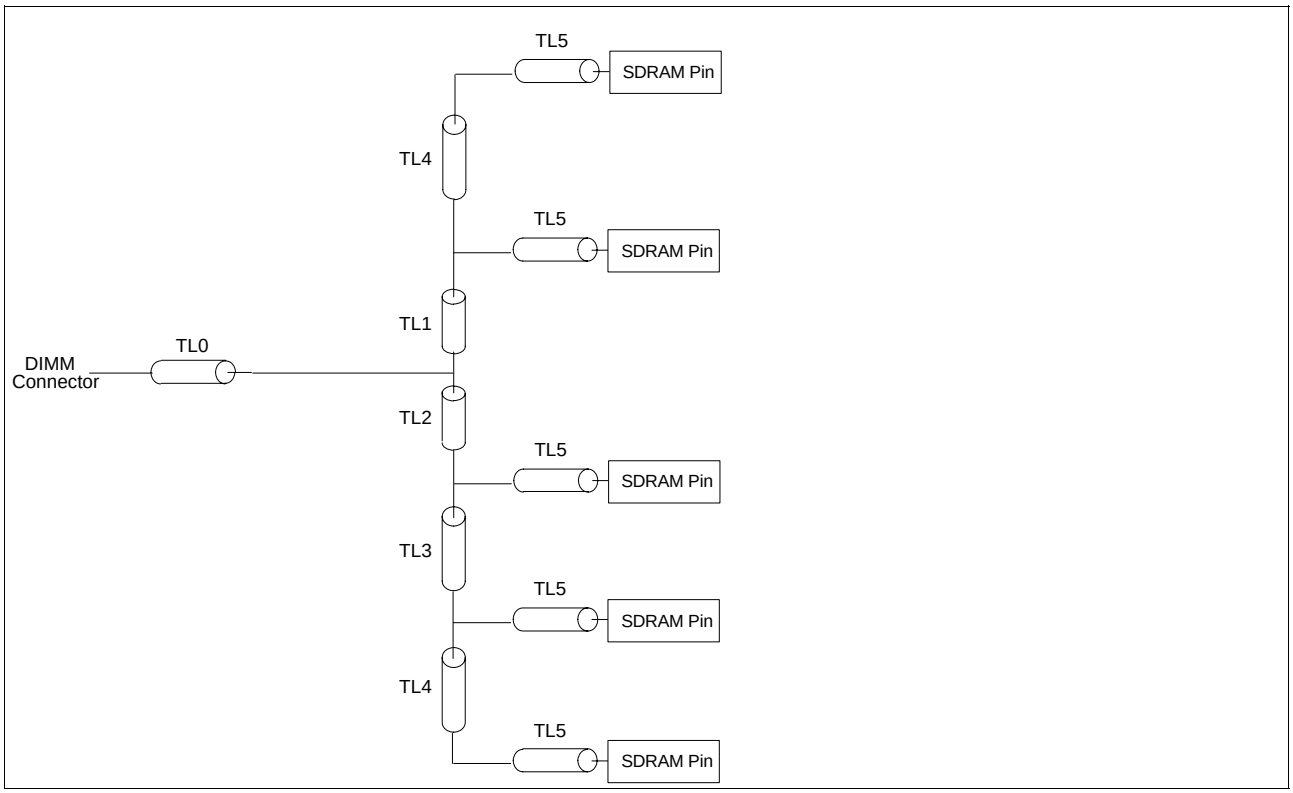
Trace Lengths for Address and Control Net Structures

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
B	.69	1.77	1.27	2.56	.40	.60	.12	.15	.41	.61	.14	.38	.49	.82	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Net Structure Routing for Address and Control (Raw Card Version C)

A, BA, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ for Raw Card Version C



Trace Lengths for Address and Control Net Structures

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
C	5.58	5.75	.91	.92	.29	.30	.62	.63	.84	.85	.07	.14	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Cross Section Recommendations

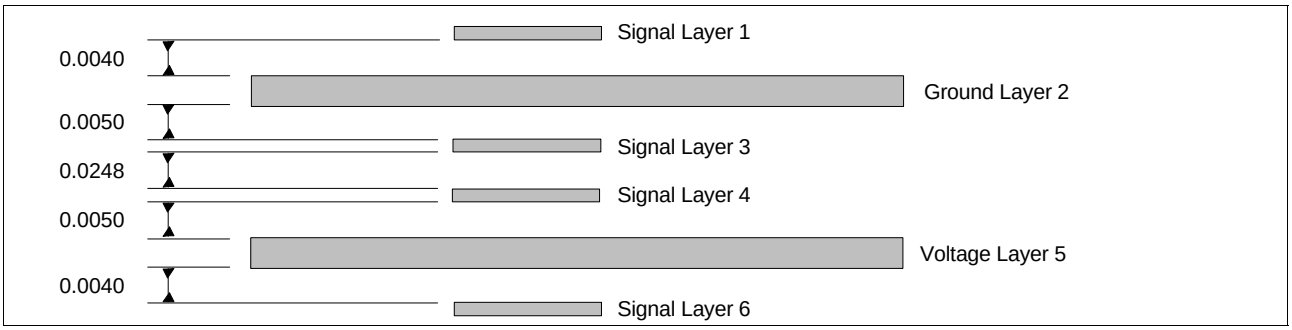
The DIMM printed circuit board design uses six-layers of glass epoxy material. PCBs must contain full ground plane and full power plane layers. The PCB stackup must be designed with 4 mil wide traces. The voltage Layer 5 is tied to all VDD and VDDQ pins on the DIMM edge connector.

Note: The PCB edge connector contacts shall be gold-plated and not chamfered.

PCB Electrical Specifications

Parameter	Min	Max	Units
Trace velocity: S0 (outer layers)	1.6	2.2	ns/ft
Trace velocity: S0 (inner layers)	2.0	2.2	ns/ft
Trace impedance: Z0 (all layers)	54	66	Ohms

Example Layer Stackup for 4 mil Traces



7. Timing Design Target

The timing for Unbuffered DDR DIMMs is critical. The following analysis should be used in order to guarantee robustly operating DIMMs.

Address setup/hold flight times

Symbol	Parameter	Time (ns) Set-up	Time (ns) Hold	Notes
t_{CO}	Clock to output (open circuit)	.75ns	-.75ns	
t_{PD}	Maximum time for the signal to propagate through the actual nets	4.6ns	1.05ns	1, 2
t_{SKEW}	Clock jitter and skew of the DIMM, system board and clock buffer	.425ns	-.35ns	
t_{SS}	Simultaneous Switch adder	.6ns	NA	3
t_{IS}	SDRAM setup/hold	1ns	.75ns (t_{IH})	
Other	brd x-talk,...	.1ns	NA	
Total		7.475ns	.7ns	

Note:

1. For set-up, 1V/ns driver, 2DIMM w/18 DRAMs each.
2. For hold, 1V/ns driver, 22 ohm series R (DIMM), 1DIMM w/4 DRAMs.
3. SSO + ISI (Intersymbol Interference) + other connector and board noise effects.

Clock Skew Contributions (t_{SKEW})

t_{SKEW} for Setup		Units		t_{SKEW} for Hold		Units
Buffer Skew	.15	ns		Buffer Skew	.15	ns
Board Skew	.10	ns		Board Skew	.10	ns
DIMM Skew	.10	ns		DIMM Skew	.10	ns
Jitter (Cyc - Cyc)	.075	ns		Total	.35	ns
Total	.425	ns				

8. Serial PD Definition

The Serial Presence Detect function MUST be implemented on the DDR SDRAM Unbuffered DIMM. The component used and the data contents must adhere to the most recent version of the JEDEC DDR Module Serial Presence Detect Specifications. Please refer to this document for all technical specifications and requirements of the Serial Presence Detect devices (Refer to JEDEC ballot JC-42.5-99-129 item 894A).

The following table is intended to be an **example** of the SPD data for a 256MB (32M x 72), 184-pin unbuffered SDRAM DDR DIMM using two physical banks of 16M x 8 PC200 devices with 12/10/2 addressing and $\overline{CAS}$ latencies of 2 and 2.5.

Serial Presence Detect Example Raw Card Version 'B'

32M x 72 DDR

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial PD Bytes Written during Production	128	80	
1	Total number of bytes in Serial PD Device	256	08	
2	Fundamental Memory Type	SDRAM DDR	07	
3	Number of Row Addresses on Assembly	12	0C	
4	Number of Column Addresses on Assembly	10	0A	
5	Number of Physical Banks on DIMM	2	02	
6	Data Width of Assembly	x72	48	
7	Data Width of Assembly (continued)	x72	00	
8	Voltage Interface Level of this Assembly	SSTL 2.5V	04	
9	SDRAM Device Cycle Time at Maximum CL (CLX = 2.5)	8.0ns	80	
10	SDRAM Device Access Time from Clock at CL = 2.5	± 0.8ns	80	
11	DIMM Configuration Type	ECC	02	
12	Refresh Rate/Type	15.6µs/SR	80	
13	Primary SDRAM Device Width	x8	08	
14	Error Checking SDRAM Device Width	x8	08	
15	SDRAM Device Attributes: Minimum Clock Delay, Random Column Access	1 Clock	01	
16	SDRAM Device Attributes: Burst Lengths Supported	2, 4, 8	0E	
17	SDRAM Device Attributes: Number of Device Banks	4	04	
18	SDRAM Device Attributes: $\overline{CAS}$ Latency	2, 2.5	0C	
19	SDRAM Device Attributes: $\overline{CS}$ Latency	0	01	
20	SDRAM Device Attributes: $\overline{WE}$ Latency	1	02	
21	SDRAM Module Attributes	Differential Clock	20	
22	SDRAM Device Attributes: General	± 0.2V$_{VDD}$	00	
23	Minimum Clock Cycle at CLX-0.5 (CL = 2)	10.0ns	A0	
24	Maximum Data Access Time (^{t}AC) from Clock at CLX-1 (CL = 1.5)	± 0.8ns	80	
25	Minimum Clock Cycle Time at CLX-1 (CL = 1.5)	N/A	00	
26	Maximum Data Access Time (^{t}AC) from Clock at CLX-1 (CL = 1.5)	N/A	00	
27	Minimum Row Precharge Time (^{t}RP)	20.0ns	50	
28	Minimum Row Active to Row Active Delay (^{t}RRD)	15.0ns	3C	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay (^{t}RCD)	20.0ns	50	
30	Minimum Active to Precharge Time (^{t}RAS)	50.0ns	32	
31	Module Bank Density	128MB	20	

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
32	Address and Command Setup Time before Clock	1.1ns	B0	
33	Address and Command Hold Time after Clock	1.1ns	B0	
34	Data/Data Mask Input Setup Time before Clock	0.6ns	60	
35	Data/Data Mask Input Hold Time after Clock	0.6ns	60	
36 - 61	Reserved	Undefined	00	
62	SPD Revision	0	00	
63	Checksum for Bytes 0 - 62	Checksum Data	cc	1
64 - 71	Manufacturers' JEDEC ID Code			
72	Module Manufacturing Location			
73 - 90	Module Part Number			
91 - 92	Module Revision Code			
93 - 94	Module Manufacturing Date	Year/Week Code	yyww	2,3
95 - 98	Module Serial Number	Serial Number	ssssssss	4
99 - 127	Reserved	Undefined	00	
128 - 255	Open for Customer Use	Undefined	00	

1. cc = Checksum Data byte, 00-FF (Hex).
2. ww = Binary coded decimal week code, 01-52 (Decimal) '01-34 (Hex).
3. yy = Binary coded decimal year code, 00-99 (Decimal) '00-63 (Hex).
4. ss = Serial number data byte, 00-FF (Hex).
5. Unused bytes are set to the value "00".
6. Unused bits in attribute bytes are set to "0".

9. Product Label

The following label should be applied to all 184pin Unbuffered DDR DIMMs, to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A minimum font size of 8 points should be used, and the number can be printed in one or more rows on the label.

Format:

PCwwwwm-aabcd-ef

Where:

wwww: Module Bandwidth
  1600: 1.6GB/sec
  2100: 2.1GB/sec
m: Module Type
  R = Registered DIMM
  U = Unbuffered DIMM (no registers on DIMM)
aa: SDRAM CAS Latency, with no decimal point (25 = 2.5CK $\overline{CAS}$ Latency)
b: SDRAM minimum t_{RCD} specification (in clocks)
c: SDRAM minimum t_{RP} specification (in clocks)
d: JEDEC SPD Revision used on this DIMM
e: Gerber file used for this design (if applicable)
  A: Reference design for R/C ”A” is used for this assembly
  B: Reference design for R/C ”B” is used for this assembly
  C: Reference design for R/C ”C” is used for this assembly
  Z: None of the ”Reference” designs were used on this assembly
f: Revision number of the reference design used:
  1: 1st revision (1st release)
  2: 2nd revision (2nd release)
  3: 3rd revision (3rd release)
  Blank: Not Applicable (used with ”Z” above)

Note: The Gerber reference designs provide as foundations for a module PCB. Manufacturers may make minor modifications to aid in manufacturability but are discouraged from making electrical changes to the design.

Example:

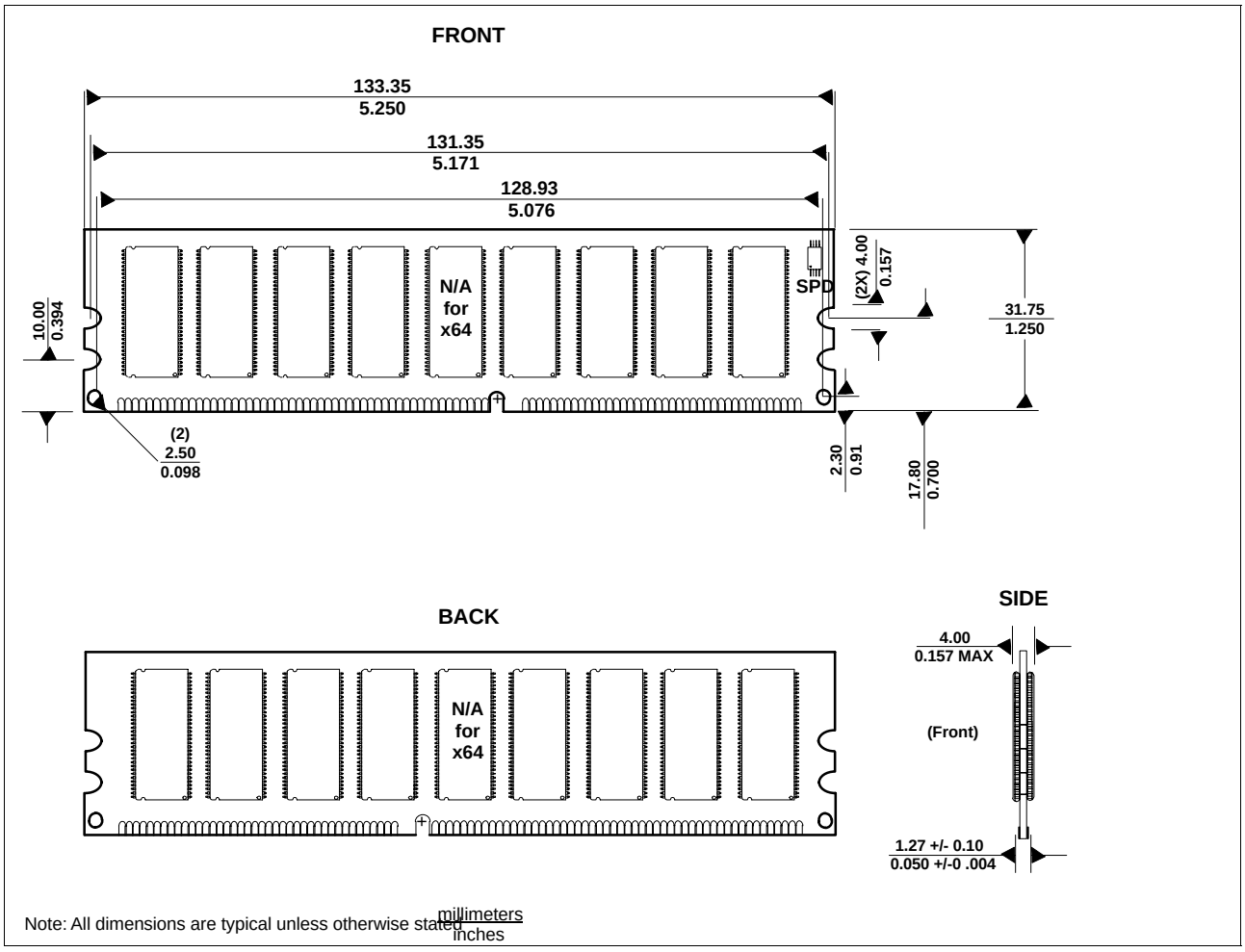
PC1600U-25330-B1 is a PC1600 DDR Unbuffered DIMM with CL = 2.5 ^{t}RCD = 3, ^{t}RP = 3 using the latest JEDEC SPD Revision 0.0 and produced based on the ”B” raw card Gerber, 1st release.

10. DIMM Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 184 Pin DIMM family. This information can be accessed on the worldwide web as follows:

1. Go to http://www.jedec.org.
2. Click on ‘Free Standards and Docs.’
3. Scroll down and double click on ‘Publication 95.’
4. Under ‘Outlines/Registrations,’ click on ‘Microelectronics Outlines.’
5. Scroll down and select ‘MO-206’ to download the PDF for this product family.

Simplified Mechanical Drawing with Keying Positions

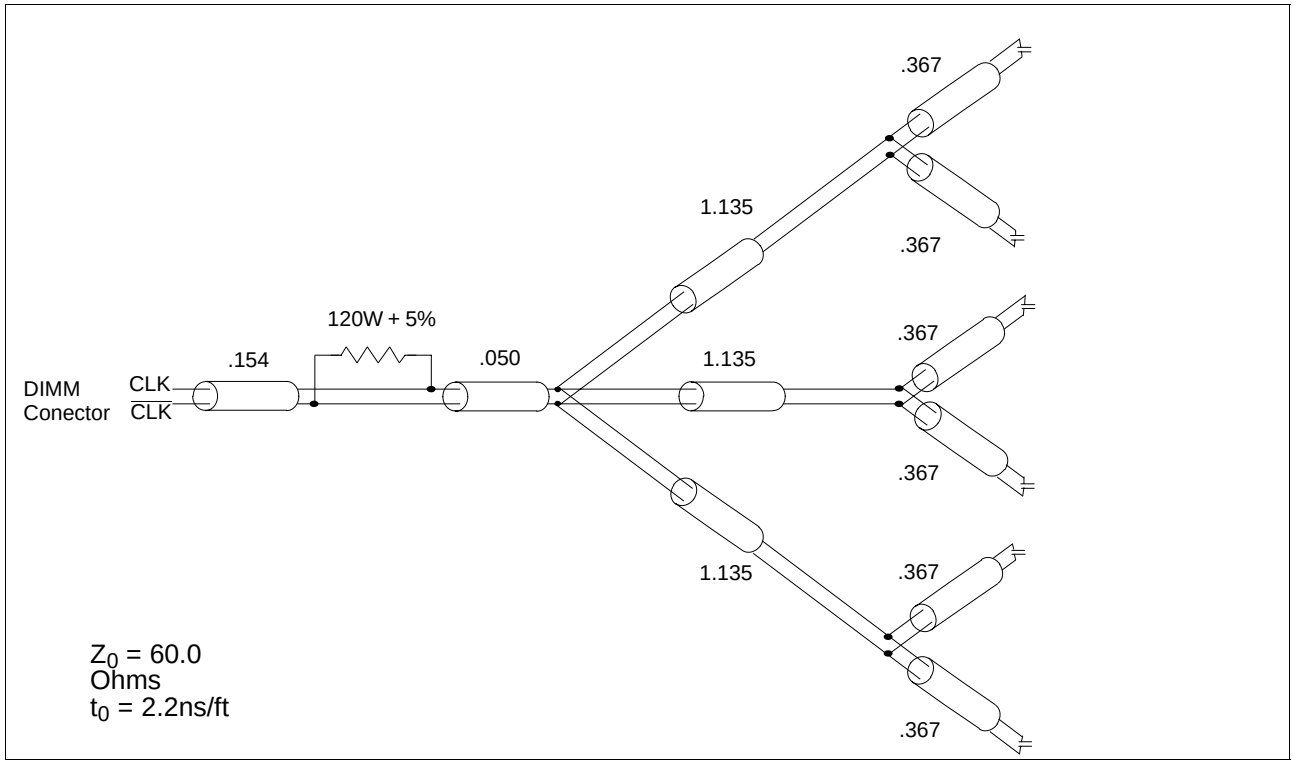


Note: The key timing in this example defines the DIMM as a 2.5V $V_{DD}/V_{DD}Q$ DDR DIMM.
*The key position defines the voltage for the DIMM: Center = 1.8 Volt $V_{DD}Q$; Left = 2.5 Volt $V_{DD}Q$; Right = 3.3 Volt $V_{DD}Q$.

11. Clocking Timing Methodology

The clock to SDRAM delay is intended to be optimized for high speed operation, while permitting a variety of component layout options. This delay should be modeled by the module supplier, to ensure accuracy, if a raw card other than one of the ”reference designs” is utilized. The clock proposed ”Reference Net” below is provided for use during module simulation to ensure an accurate clock delay.

Unbuffered DIMM Differential Clock Reference Net



Notes: 1. Capacitor value equals 1/2 the nominal SDRAM input capacitance.
2. Lengths in inches.